

LCFC Confidential


G Project M/B Schematics Document

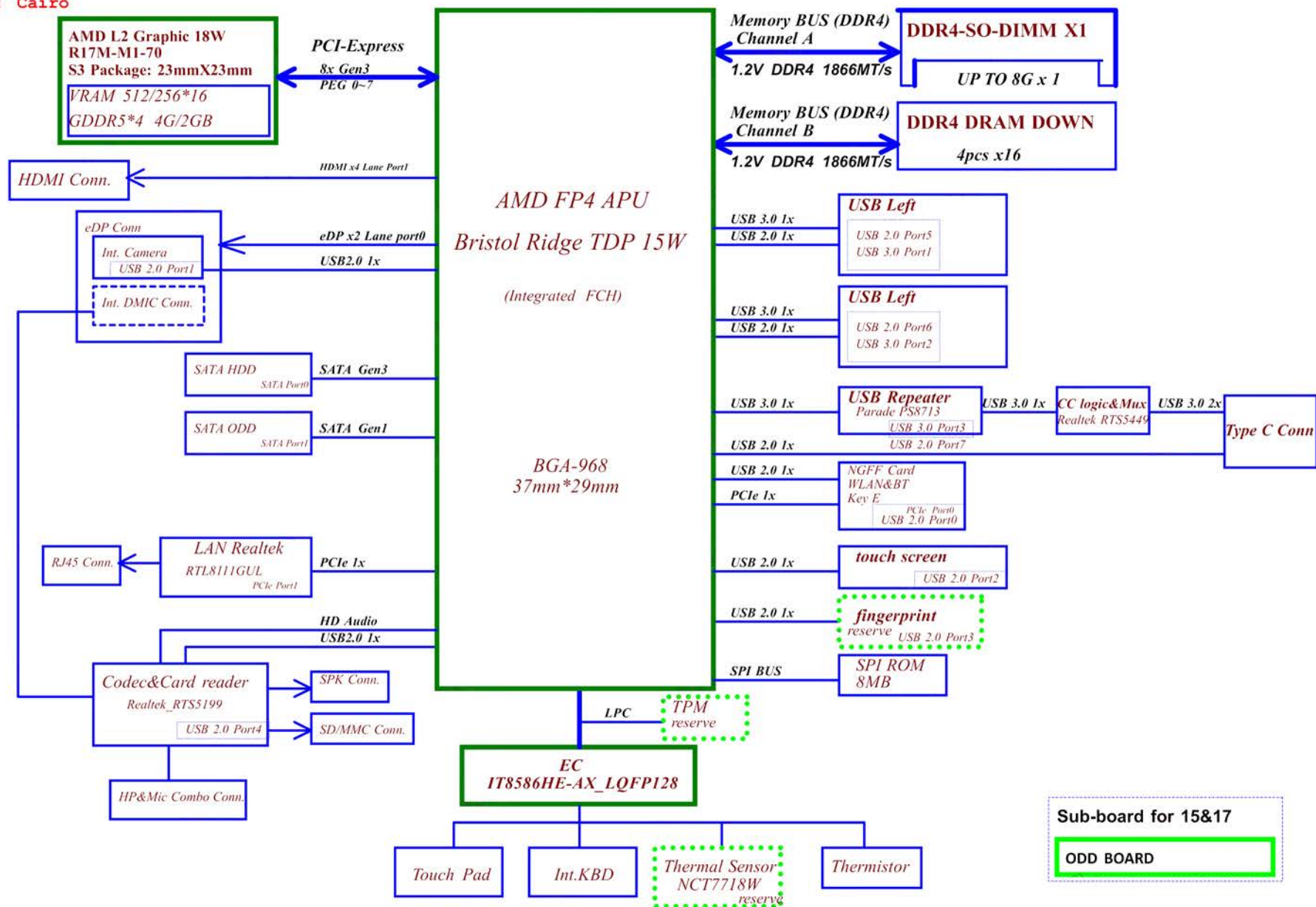
AMD FP4 Bristol Ridge SOC with DDRVI

AMD R17M-M1-70

2016-11-09

REV: 0.1

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/15	Deciphered Date	2013/08/15	Cover Page		
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Title	Block Diagram		
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State \ power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+1.2V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +2.5VS +APU_CORE_N +APU_CORE_N +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

DRAM Config.	BOARD ID0 API08	BOARD ID1 AGPIO10	BOARD ID2 AGPIO16 internal pull up 40
	0: 14''	0: Dis	0: No KBL
	1: 15''	1: UMA	0: KBL

USB 2.0	USB 3.0	Port	Port device
EHCI0		0	Blue Tooth
		1	Camera
		2	Touch screen
		3	Finger print
xHCI	0	4	Card Reader USB 2.0 bus
	1	5	LEFT USB (3.0) 1#
	2	6	LEFT USB (3.0) 2#
	3	7	Type C

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	GPU
	1	
	2	
	3	
	4	
	5	
	6	
	7	

	SOURCE	GPU	BATT	IT8586	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8586 +3VL	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586 +3VL	X	X		X	X	X	X	X	V
EC_SMB_CK3 EC_SMB_DA3	IT8586 +3VS	V +3VS_VGA	X		X	X	V	V 1.8VS	X	X
APU_SCLK0 APU_SDAT0	APU +3VS	X	X	X	V	V	X		X	X


	SOURCE	Device
TP_I2C0_SCL	APU	Touch Pad
TP_I2C0_SDA	+1.8VS	3VS

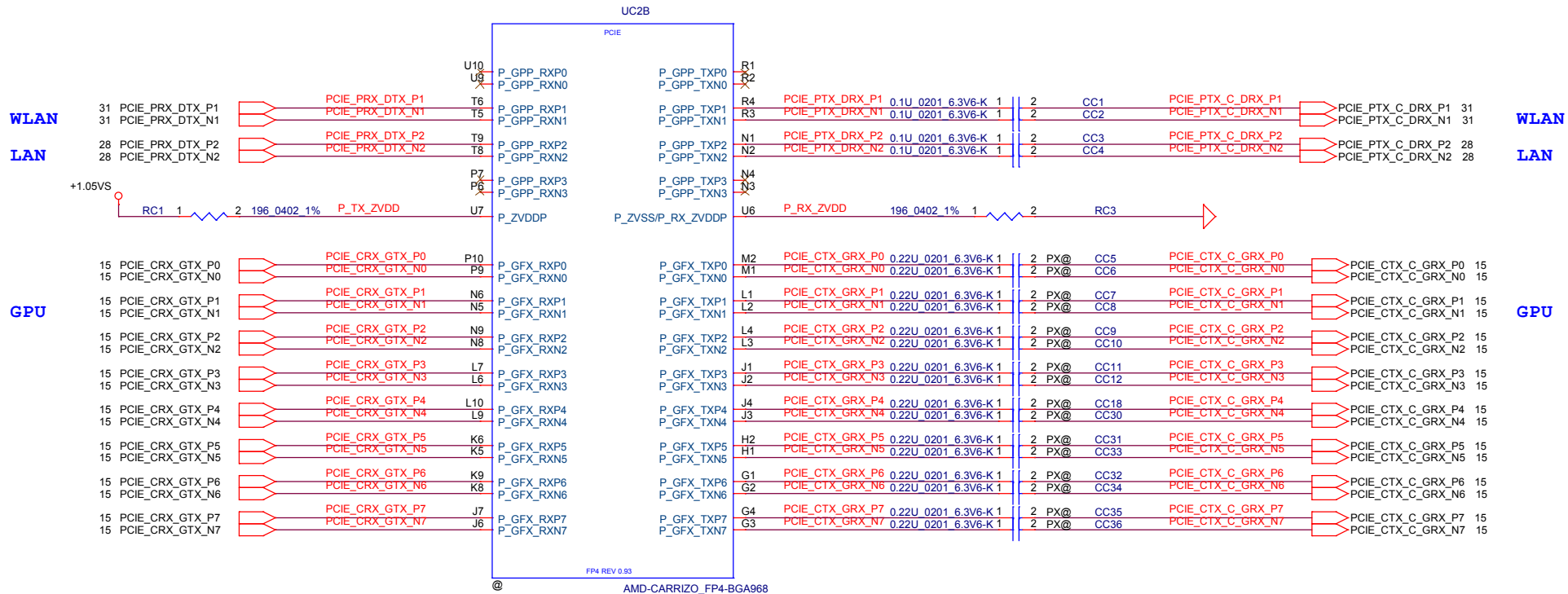
Device	Address
Elan: SA469D 22 HA 69x104x1 0	?
Synaptics: T M P3255-008 69x104x1 0	?


BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_14@	EMC 14 part
EMC_15@	EMC 15 part
RF@	RF Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
KBL@	keyboard backlight part
HDT@	HDT Debug part
BR@	Bristol Ridge Part
ST@	Stoney Ridge part
BRPX@	Bristol Ridge Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
HDMI@	HDMI Logo

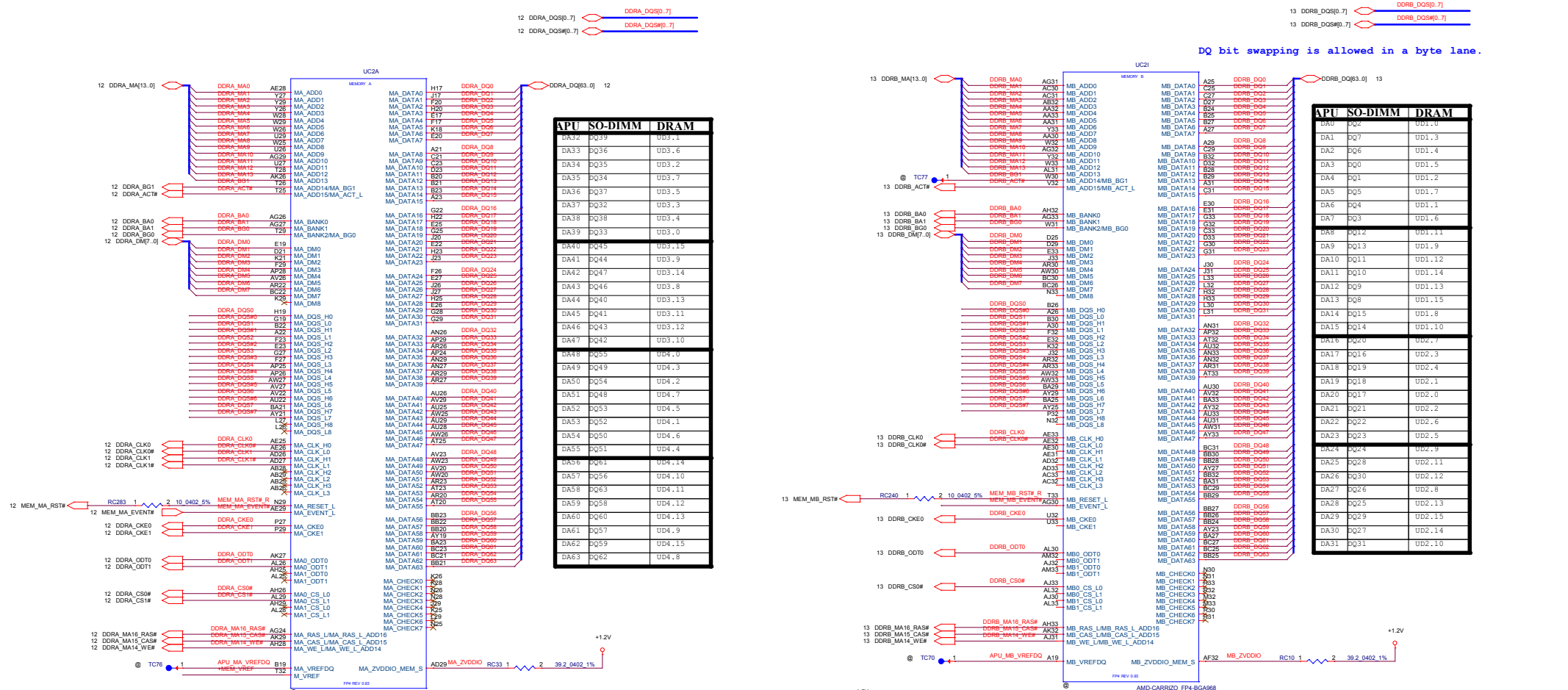
Device	Address	Device	Address	Device	Address
Battery	0X16	PMIC	?	Thermal Sensor	1001_100xb(reserve)
Charger	0001 0010 b			GPU	0x41(default)
				APU SB-TSI	relate to F3x1E4(SbiAddr) or Address Select Pins setting

Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

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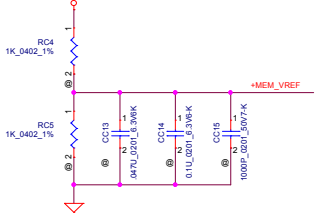



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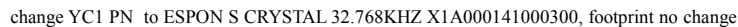
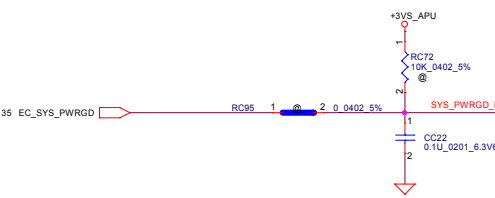


SO-DIMM

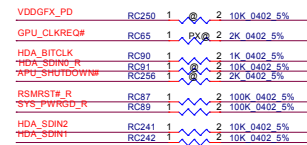
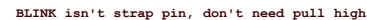
Memory down



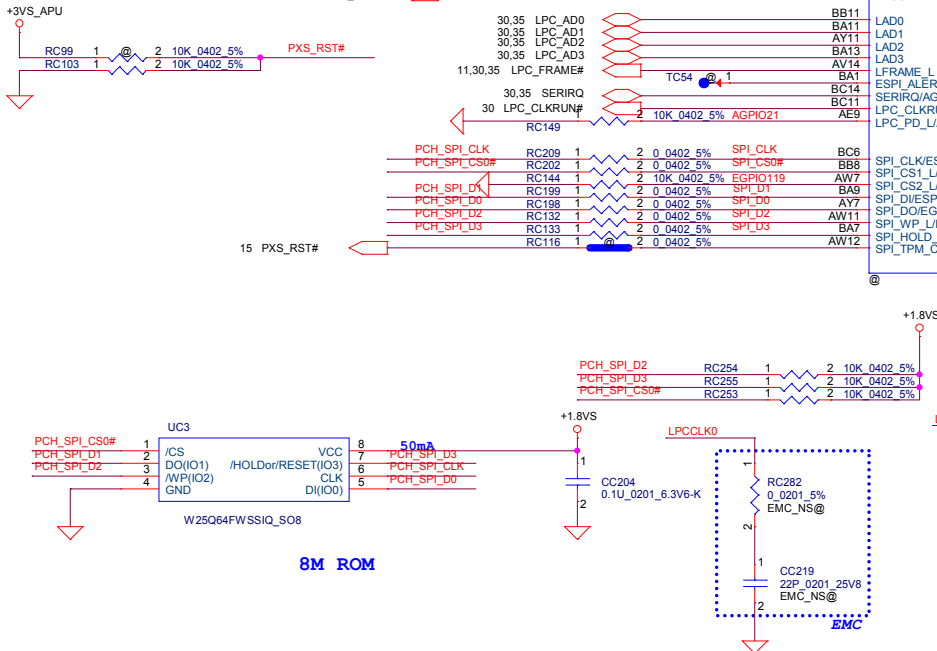
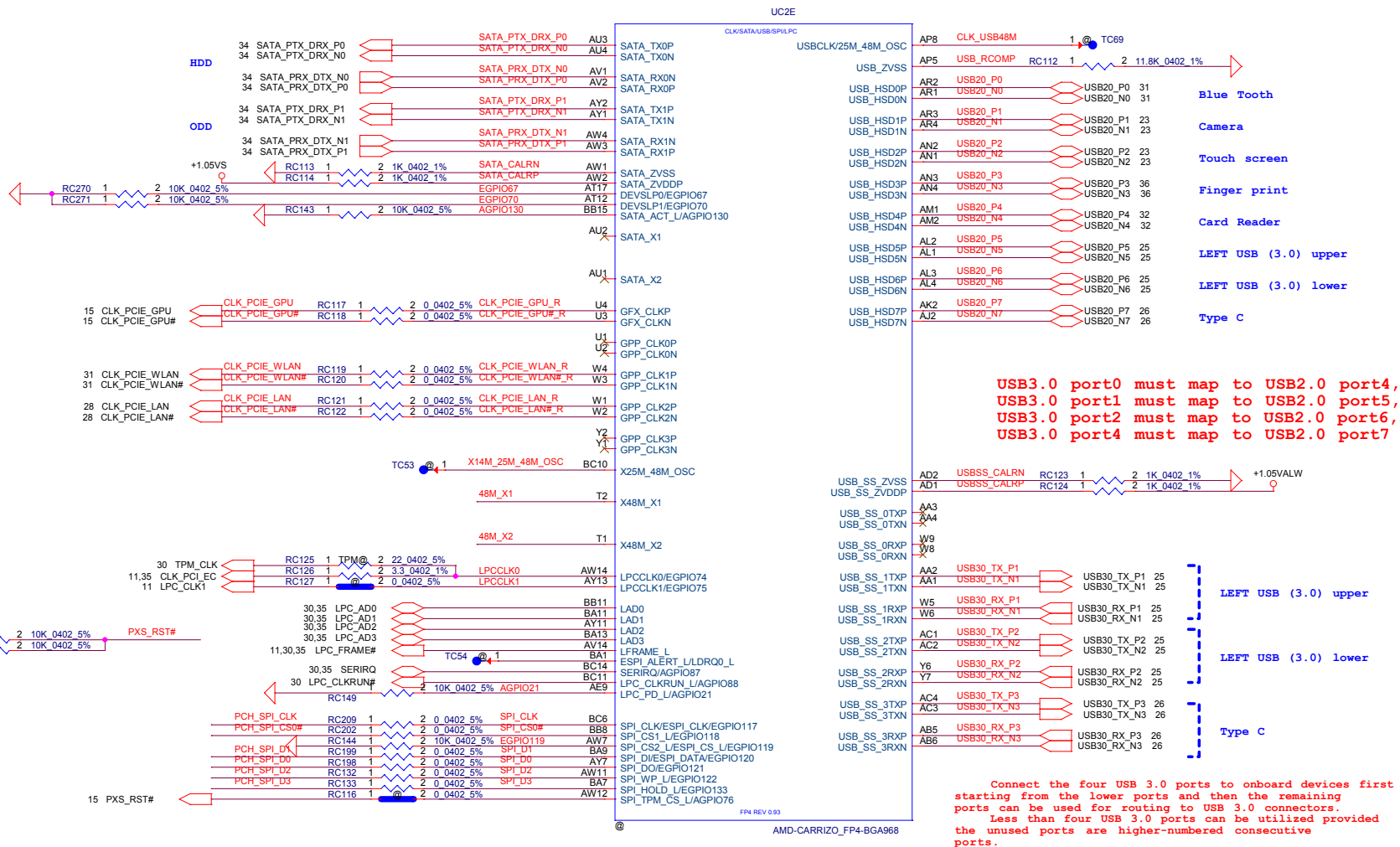
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	FP4 (MEM)	
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BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
BOARD_ID5
BOARD_ID6



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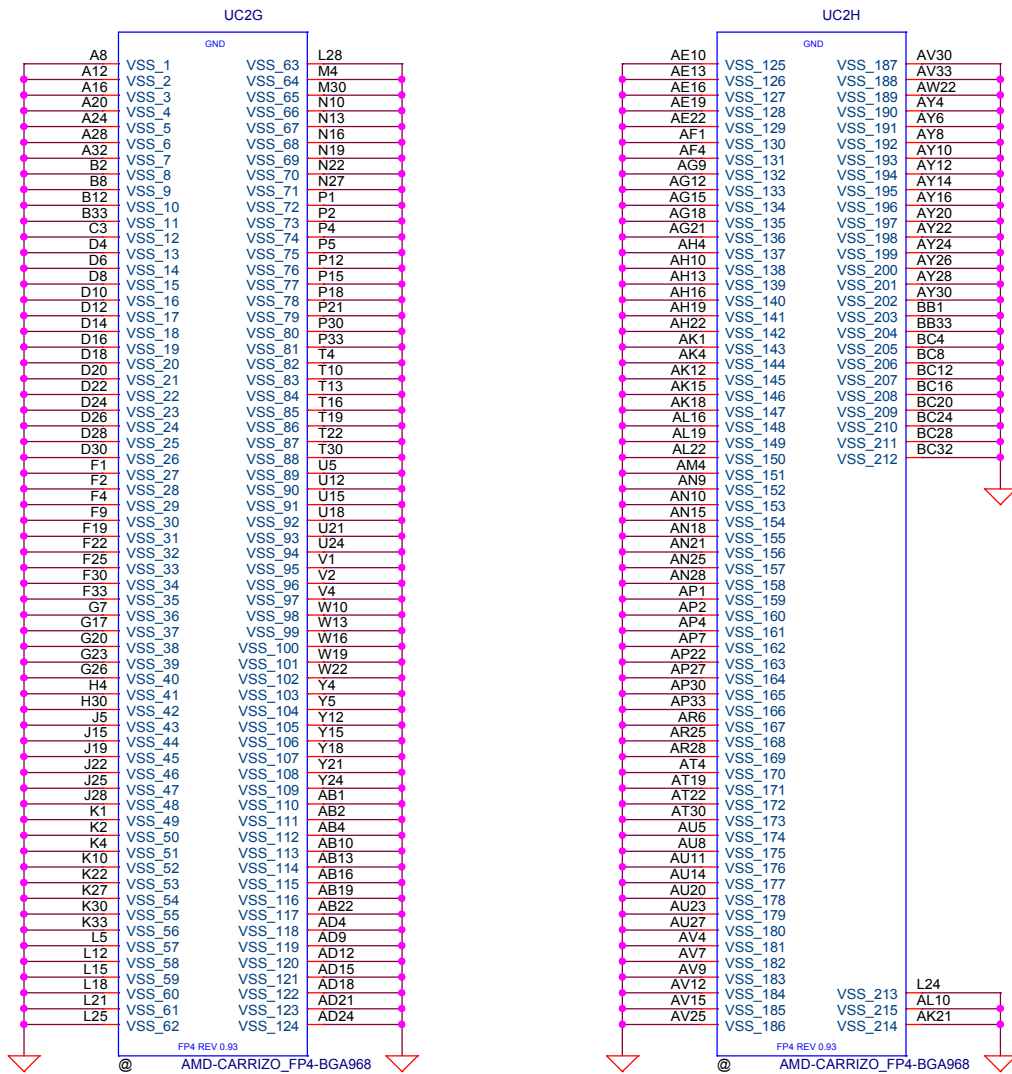


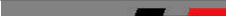
CC219 and CC218 should 27pf as EMC suggest

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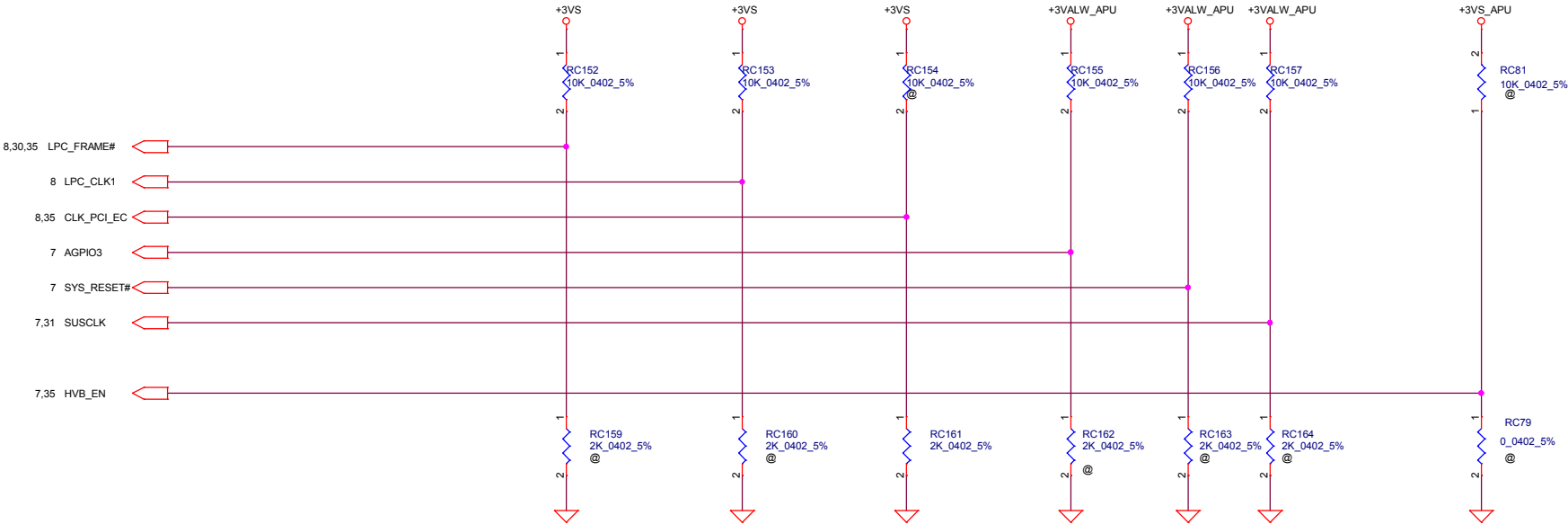


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STRAP PINS



Signal	LFRAME_L	LPCCCLK1	LPCCCLK0	RTCCLK Int pull-up	SYS_RESET_L Int pull-up	AGPIO3 Int pull-up	HVB_EN
Type	II	II	II	I	I	I	
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	RTC Coin Battery is implemented Default	Normal Power Up &Reset Timing Default	Enhanced reset logic (for quicker S5 resume) Default	floating Disable HVB on FP4 platforms Default
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	RTC Coin Battery is not implemented	Reserved	traditional reset logic	connected to VSS Enable HVB on FP4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

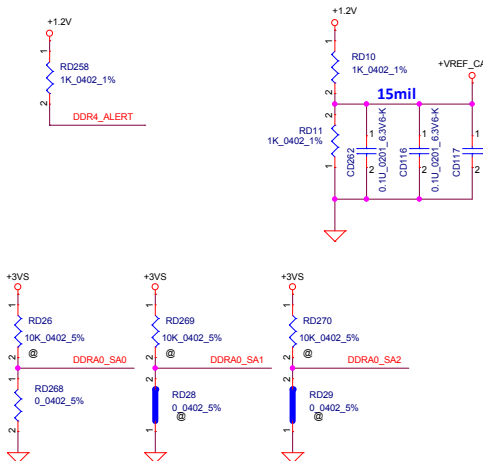
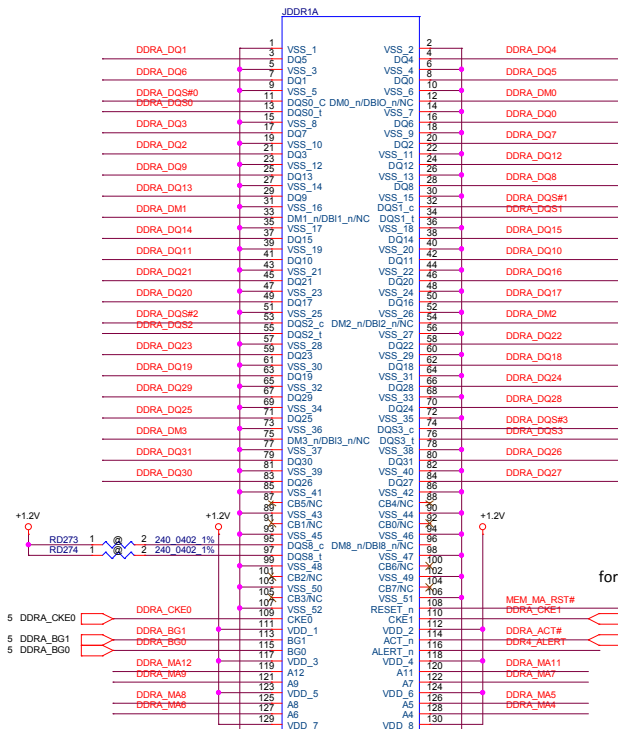
Type II straps become valid after PWR_GOOD is asserted,straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.

Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

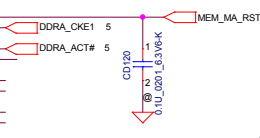
If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to `1` for & AGPIO3

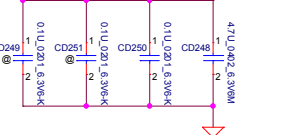


for MEM_MB_RST# overshoot issue

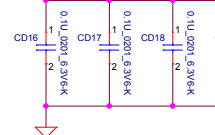


Layout Note: Place near JDDR1

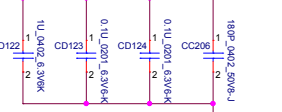
follow CRB 1pcs 4.7uf + 1pcs 0.1uf



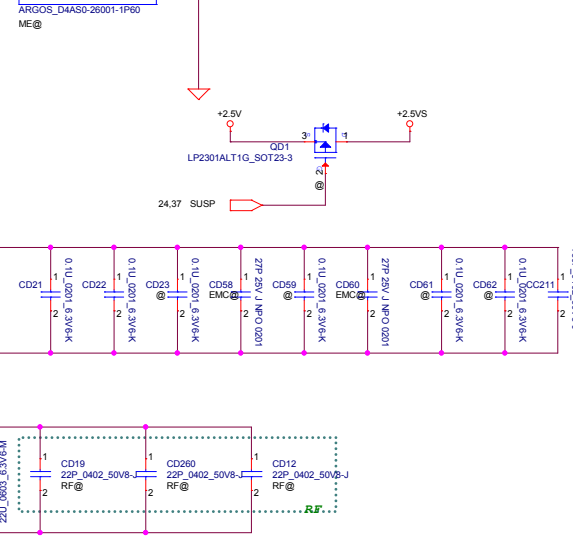
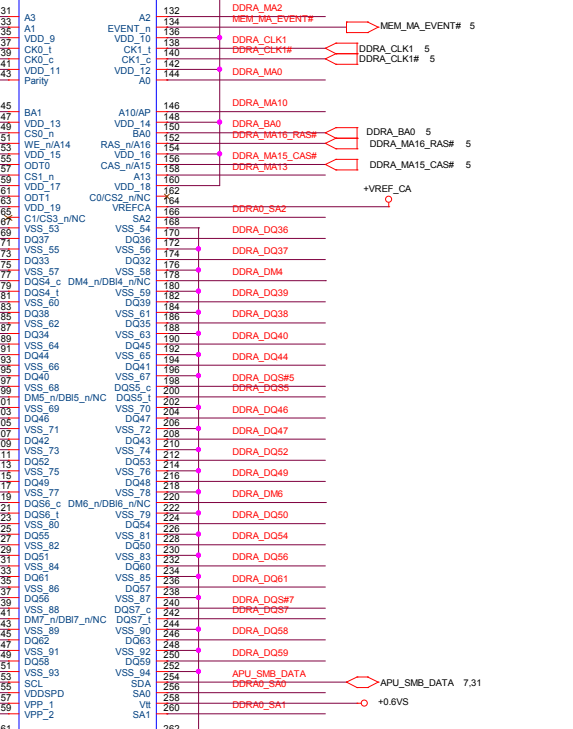
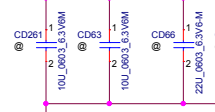
follow CRB 6pcs 0.1uf



follow CRB 1pcs 1uf + 2pcs 0.1uf + 1pcs 180pf

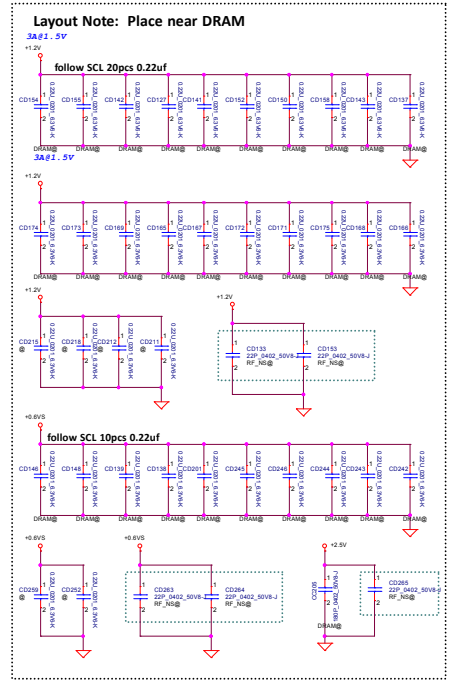
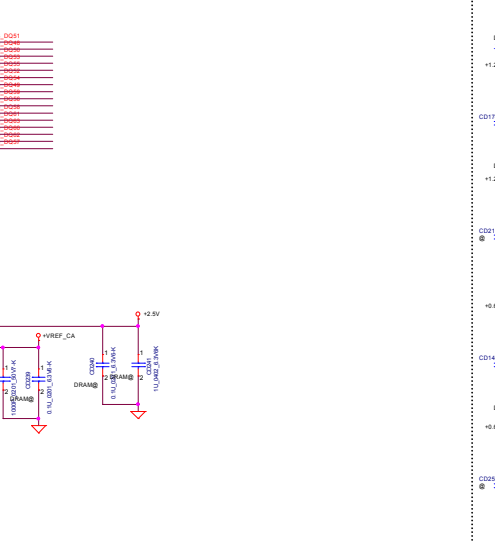
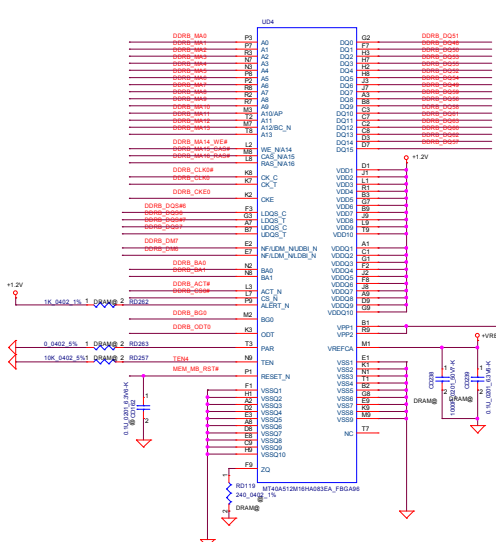
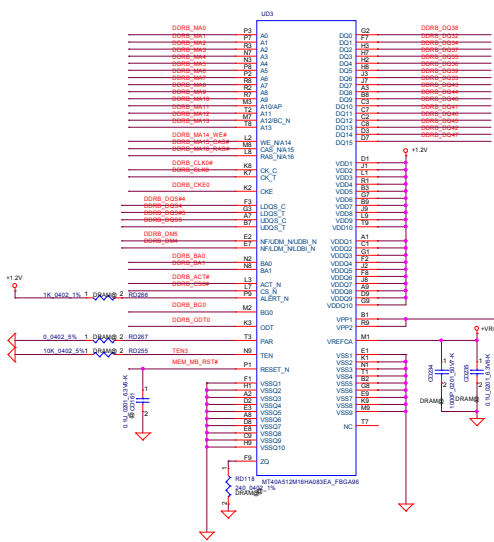


follow CRB 6pcs 0.1uf



Swap Table

Pin Name	Net Name
DQ0	DBRB_DQ6
DQ1	DBRB_DQ5
DQ2	DBRB_DQ3
DQ3	DBRB_DQ7
DQ4	DBRB_DQ4
DQ5	DBRB_DQ0
DQ6	DBRB_DQ1
DQ7	DBRB_DQ2
DQS#0	DBRB_DQS#0
DQS0	DBRB_DQS0
DQ8	DBRB_DQ8
DQ9	DBRB_DQ13
DQ10	DBRB_DQ11
DQ11	DBRB_DQ10
DQ12	DBRB_DQ12
DQ13	DBRB_DQ9
DQ14	DBRB_DQ15
DQ15	DBRB_DQ14
DQS#1	DBRB_DQS#1
DQS1	DBRB_DQS1
DQ16	DBRB_DQ20
DQ17	DBRB_DQ16
DQ18	DBRB_DQ18
DQ19	DBRB_DQ19
DQ20	DBRB_DQ17
DQ21	DBRB_DQ21
DQ22	DBRB_DQ22
DQ23	DBRB_DQ23
DQS#2	DBRB_DQS#2
DQS2	DBRB_DQS2
DQ24	DBRB_DQ28
DQ25	DBRB_DQ25
DQ26	DBRB_DQ31
DQ27	DBRB_DQ27
DQ28	DBRB_DQ24
DQ29	DBRB_DQ29
DQ30	DBRB_DQ26
DQ31	DBRB_DQ30
DQS#3	DBRB_DQS#3
DQS3	DBRB_DQS3
DQ32	DBRB_DQ33
DQ33	DBRB_DQ37
DQ34	DBRB_DQ34
DQ35	DBRB_DQ38
DQ36	DBRB_DQ36
DQ37	DBRB_DQ32
DQ38	DBRB_DQ35
DQ39	DBRB_DQ39
DQS#4	DBRB_DQS#4
DQS4	DBRB_DQS4
DQ40	DBRB_DQ45
DQ41	DBRB_DQ44
DQ42	DBRB_DQ46
DQ43	DBRB_DQ42
DQ44	DBRB_DQ41
DQ45	DBRB_DQ40
DQ46	DBRB_DQ47
DQ47	DBRB_DQ43
DQS#5	DBRB_DQS#5
DQS5	DBRB_DQS5
DQ48	DBRB_DQ49
DQ49	DBRB_DQ48
DQ50	DBRB_DQ54
DQ51	DBRB_DQ55
DQ52	DBRB_DQ53
DQ53	DBRB_DQ52
DQ54	DBRB_DQ50
DQ55	DBRB_DQ51
DQS#6	DBRB_DQS#6
DQS6	DBRB_DQS6
DQ56	DBRB_DQ60
DQ57	DBRB_DQ56
DQ58	DBRB_DQ63
DQ59	DBRB_DQ59
DQ60	DBRB_DQ61
DQ61	DBRB_DQ57
DQ62	DBRB_DQ58
DQ63	DBRB_DQ62
DQS#7	DBRB_DQS#7
DQS7	DBRB_DQS7



Pin	File Name	Host Name
Q00	D00R Q03	
Q01	D00R Q04	
Q02	D00R Q05	
Q03	D00R Q06	
Q04	D00R Q07	
Q05	D00R Q08	
Q06	D00R Q09	
Q07	D00R Q10	
Q08R0	D00R Q08R0	
Q090	D00R Q090	
UD1		
Q08	D00R Q08	
Q09	D00R Q09	
Q10	D00R Q10	
Q11	D00R Q11	
Q12	D00R Q12	
Q13	D00R Q13	
Q14	D00R Q14	
Q15	D00R Q15	
Q16	D00R Q16	
UD1		
Q016	D00R Q07	
Q017	D00R Q08	
Q018	D00R Q09	
Q019	D00R Q10	
Q020	D00R Q11	
Q021	D00R Q12	
Q022	D00R Q13	
Q023	D00R Q14	
Q024	D00R Q15	
Q025R2	D00R Q08R2	
Q082	D00R Q082	
UD2		
Q024	D00R Q15	
Q025	D00R Q16	
Q026	D00R Q17	
Q027	D00R Q18	
Q028	D00R Q19	
Q029	D00R Q20	
Q030	D00R Q21	
Q031	D00R Q22	
Q032	D00R Q23	
Q033	D00R Q24	
Q034	D00R Q25	
Q035R3	D00R Q08R3	
Q083	D00R Q083	
UD2		
Q032	D00R Q23	
Q033	D00R Q24	
Q034	D00R Q25	
Q035	D00R Q26	
Q036	D00R Q27	
Q037	D00R Q28	
Q038	D00R Q29	
Q039	D00R Q30	
Q040R4	D00R Q08R4	
Q084	D00R Q084	
UD3		
Q040	D00R Q30	
Q041	D00R Q31	
Q042	D00R Q32	
Q043	D00R Q33	
Q044	D00R Q34	
Q045	D00R Q35	
Q046	D00R Q36	
Q047	D00R Q37	
Q048	D00R Q38	
Q049R5	D00R Q08R5	
Q085	D00R Q085	
UD		
Q048	D00R Q38	
Q049	D00R Q39	
Q050	D00R Q40	
Q051	D00R Q41	
Q052	D00R Q42	
Q053	D00R Q43	
Q054	D00R Q44	
Q055	D00R Q45	
Q056R6	D00R Q08R6	
Q086	D00R Q086	
UD4		
Q050	D00R Q39	
Q051	D00R Q40	
Q052	D00R Q41	
Q053	D00R Q42	
Q054	D00R Q43	
Q055	D00R Q44	
Q056	D00R Q45	
Q057	D00R Q46	
Q058R7	D00R Q08R7	
Q087	D00R Q087	
UD4		

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

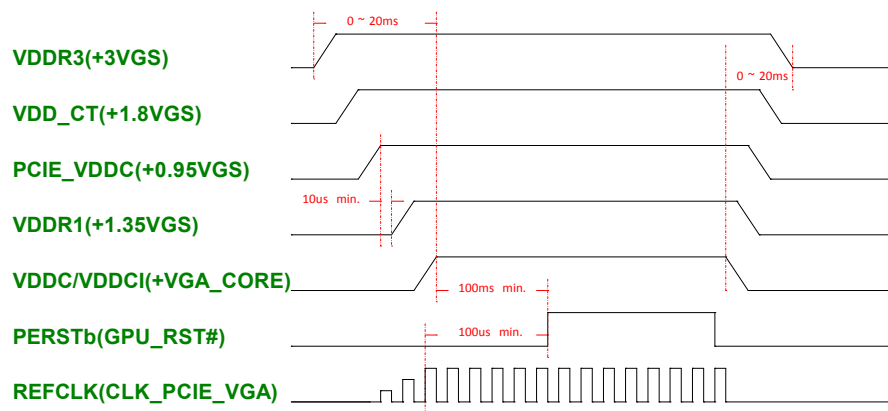
It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

The gate circuits must meet the slew rate requirement (such as \leq 50 mV/ μ s).

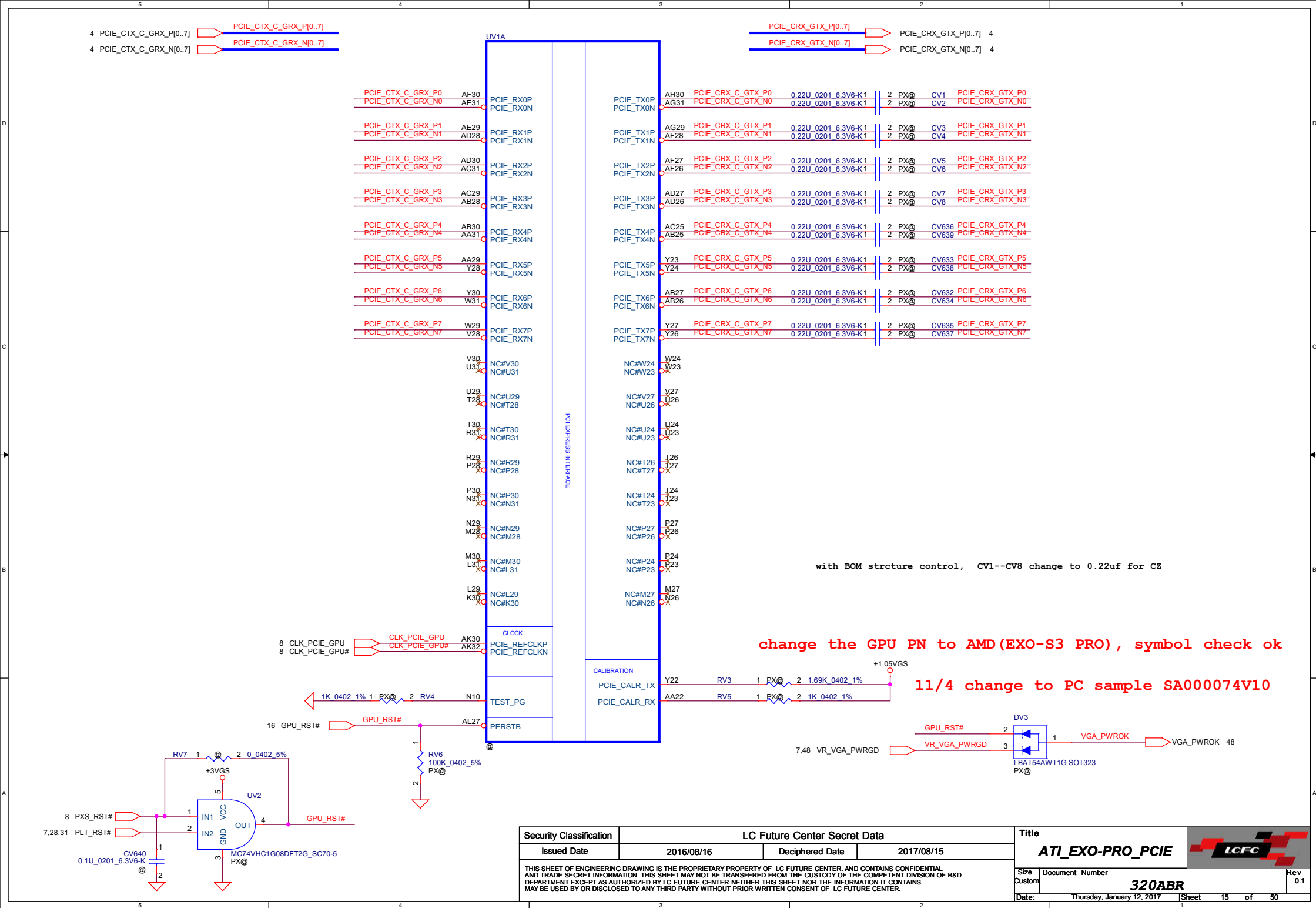
For power down, reversing the ramp-up sequence is recommended.




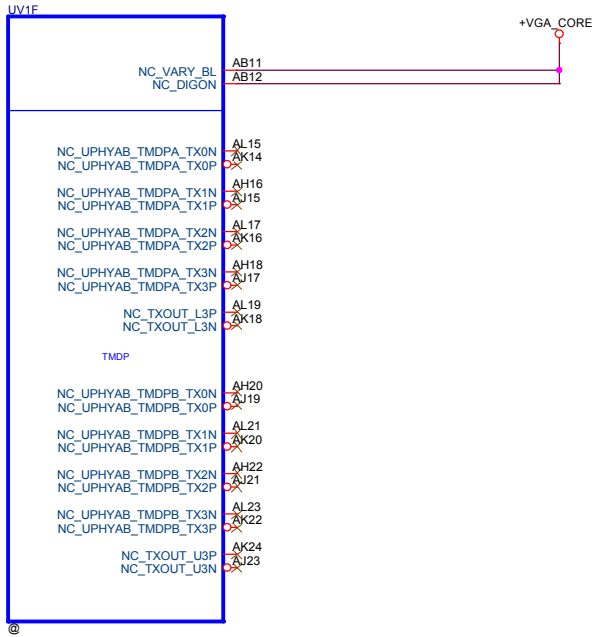
VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
4Gb GDDR5 256M x 16	Hynix H5GC4H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron EDW4032BABG-70-F 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G41325FE-HC28 6.0Gbps@1.35V	110	3.4K	10K
8Gb GDDR5 512M x 16	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70-A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

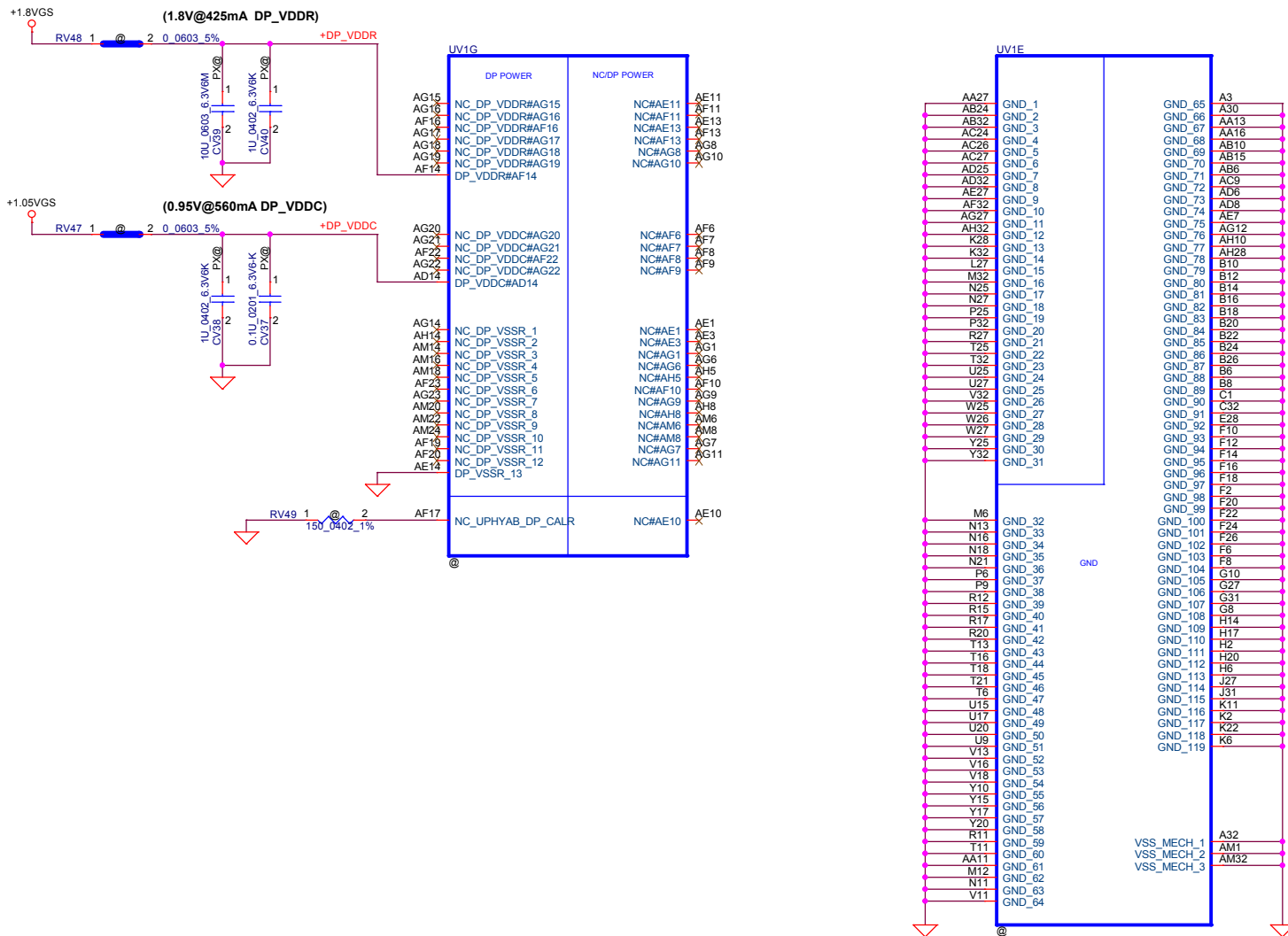
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Issued Date		2016/08/16		Deciphered Date	
2016/08/16		2017/08/15		VGA Notes List	
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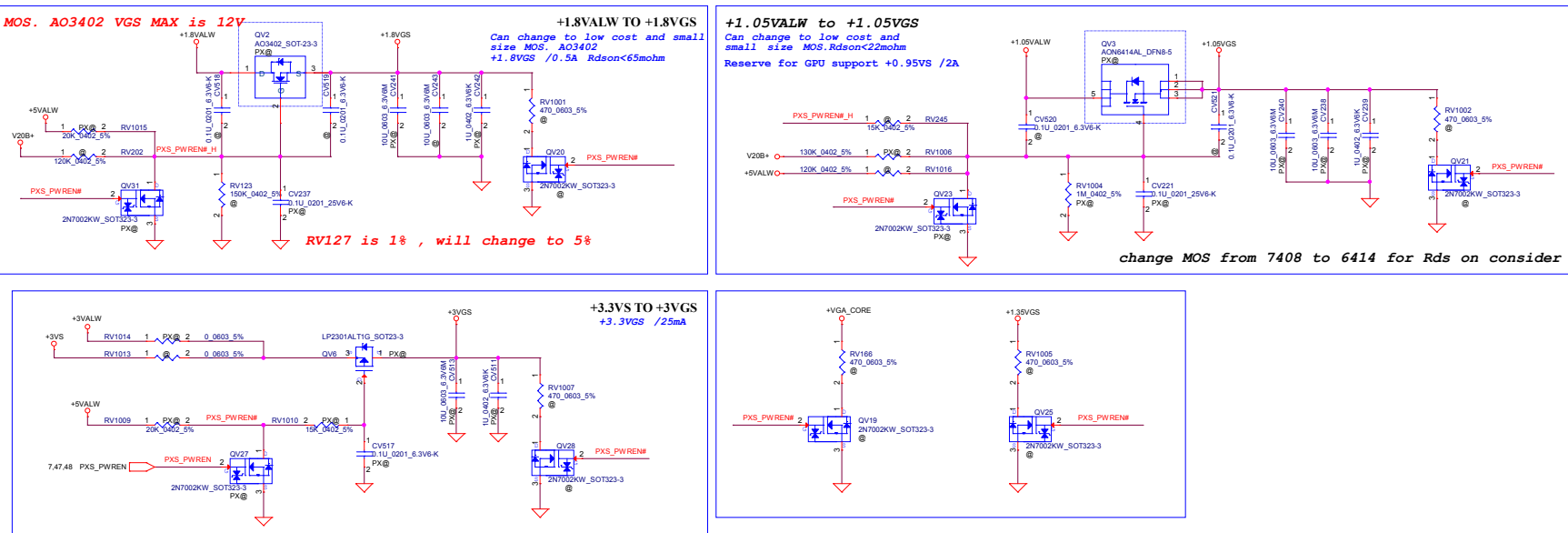
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				Date: Thursday, January 12, 2017	Rev 0.1
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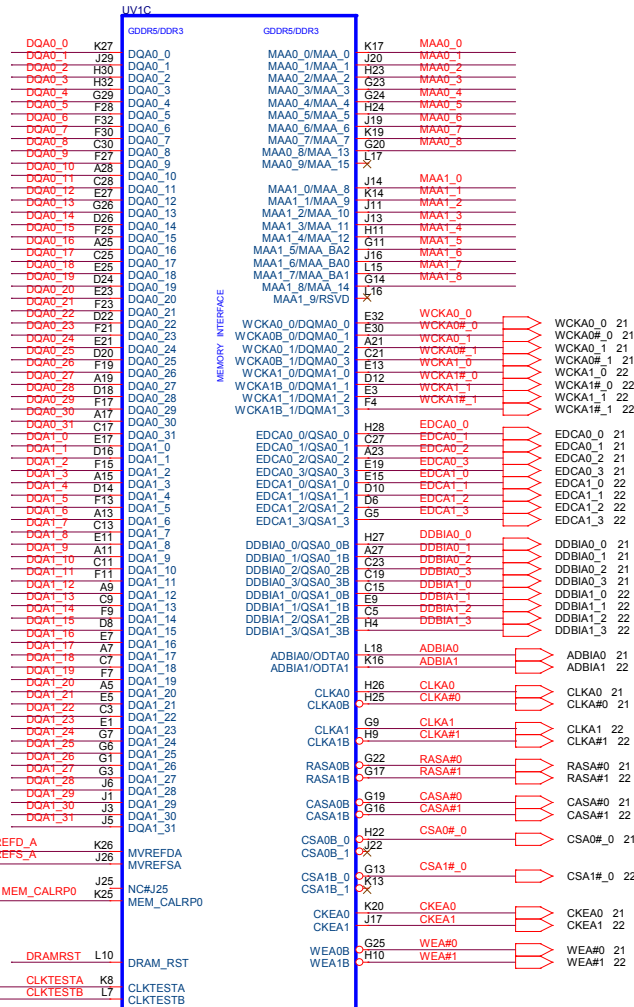
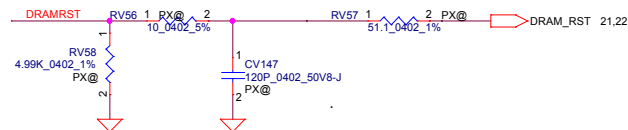
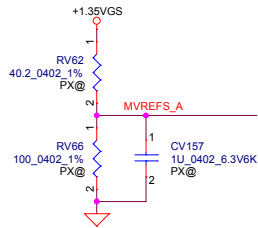
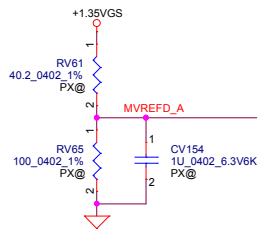
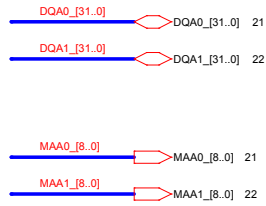


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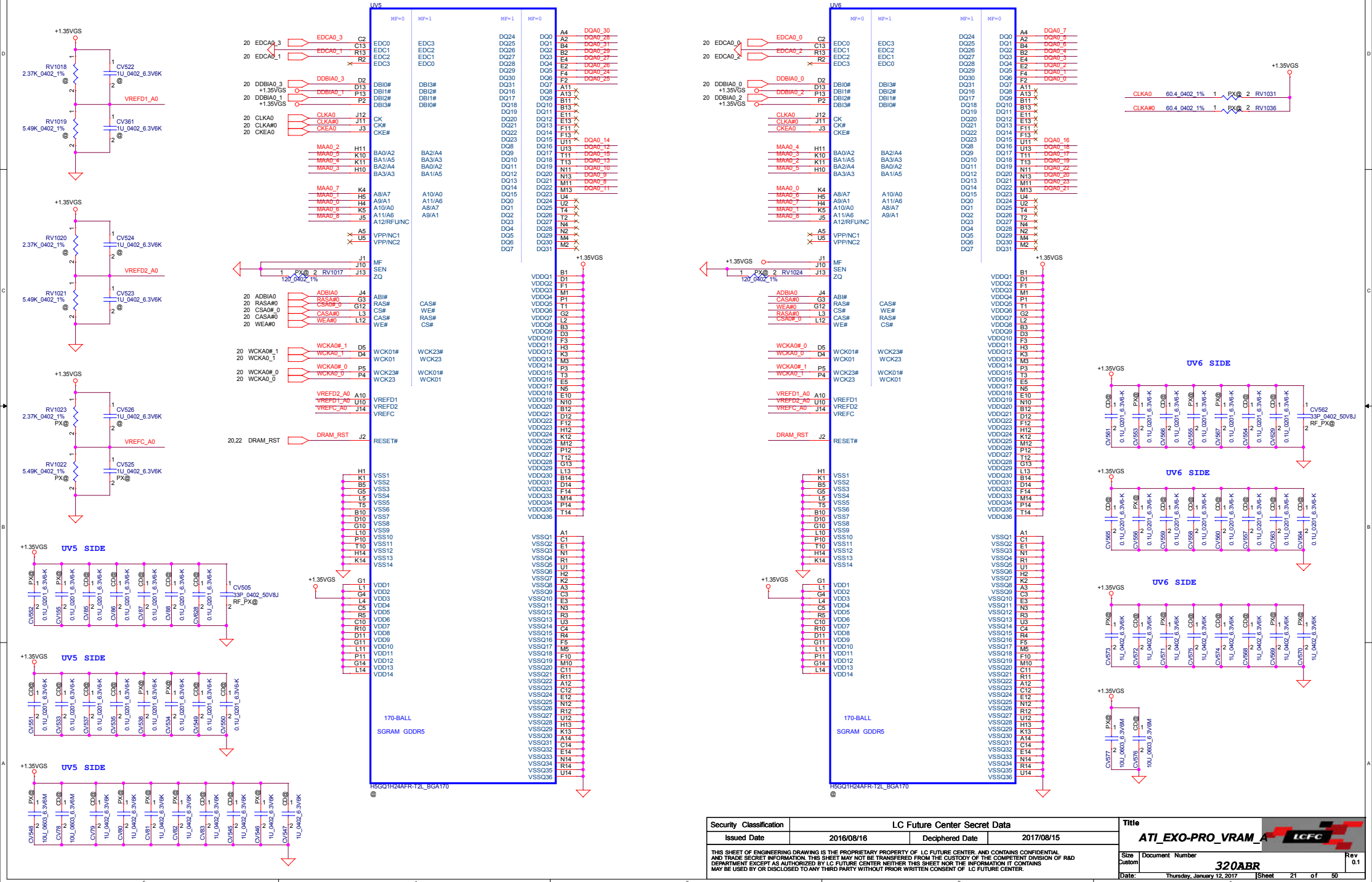
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				Sheet 20	of 50

Lower 32 bits

DQA0[31..0] 20
MAA0[8..0] 20

MF=0 No Mirror

MF=1 Mirror



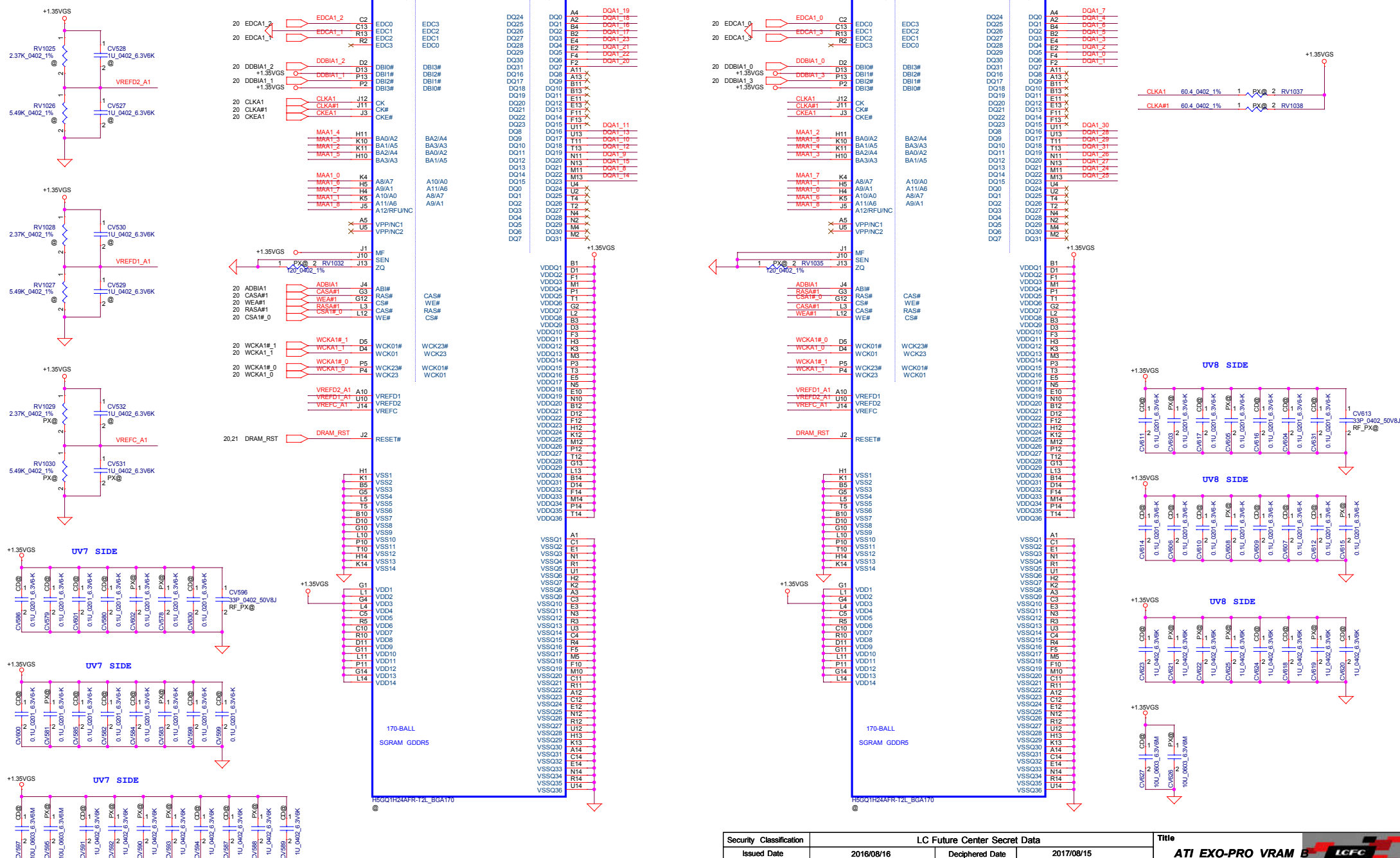
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Date:		Thursday, January 12, 2017		Sheet	21 of 50

Upper 32 bits

DQA1_[31..0] 20
MAA1_[8..0] 20

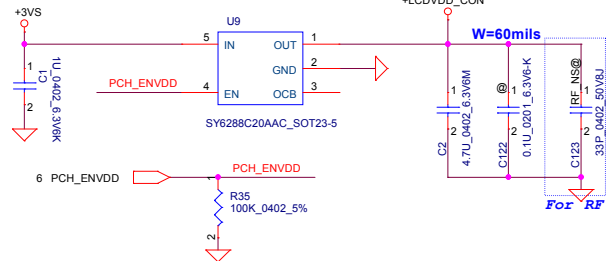
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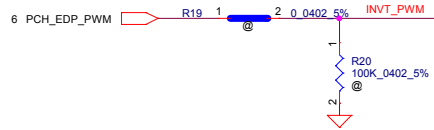


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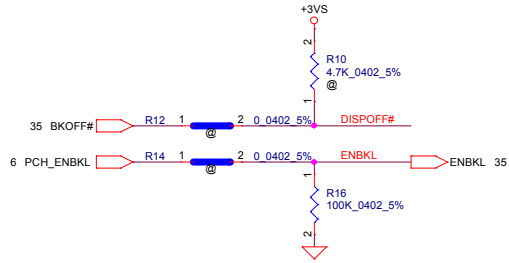
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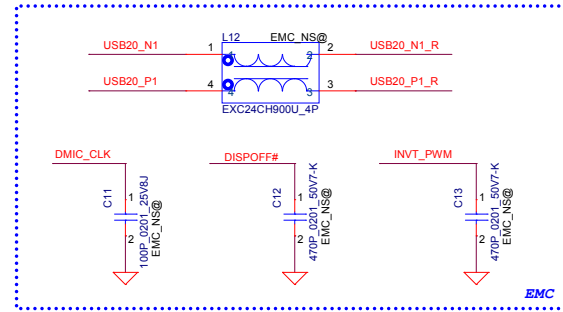
APU output enable Voh min is 1.8V-0.45V=1.35V



Need Short

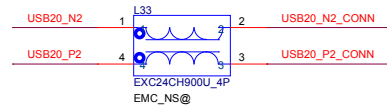


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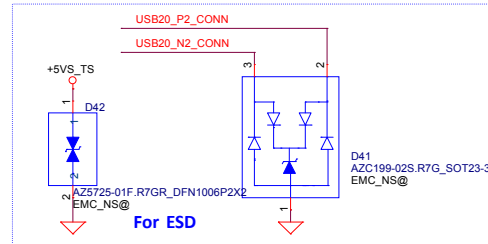


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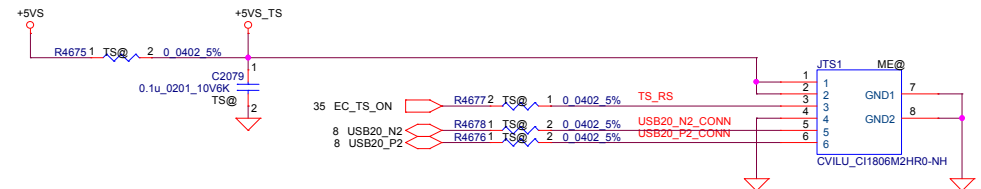
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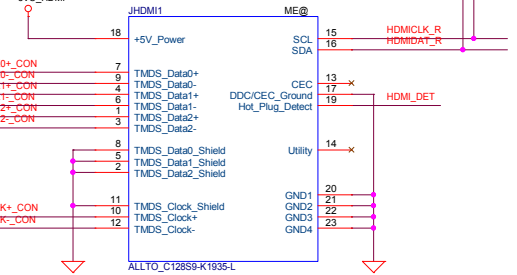
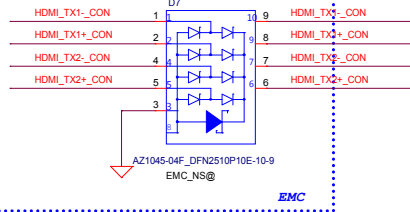
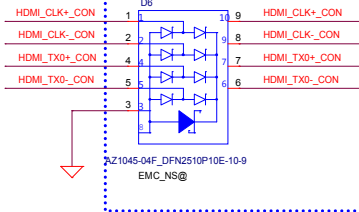
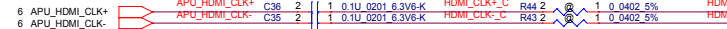
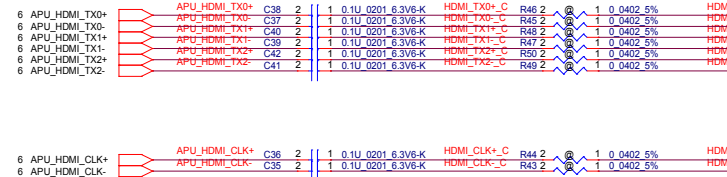
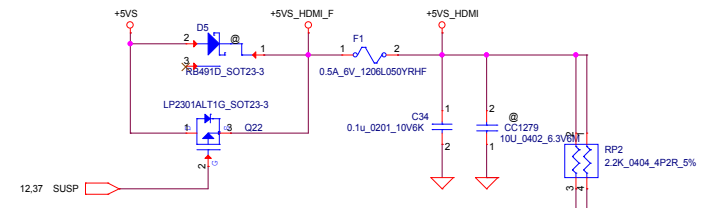
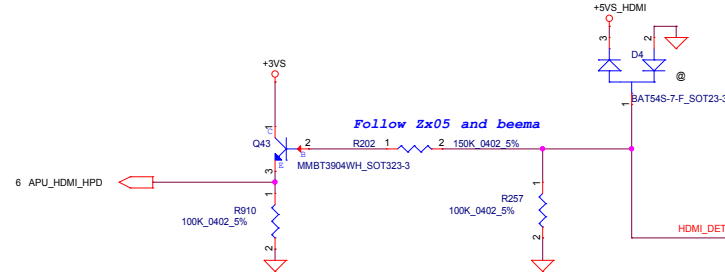
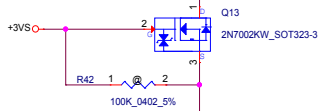
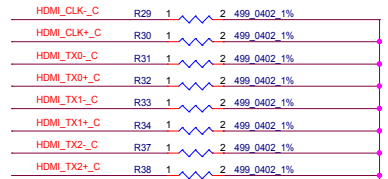
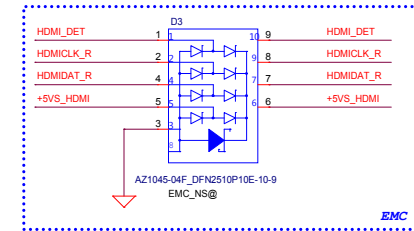
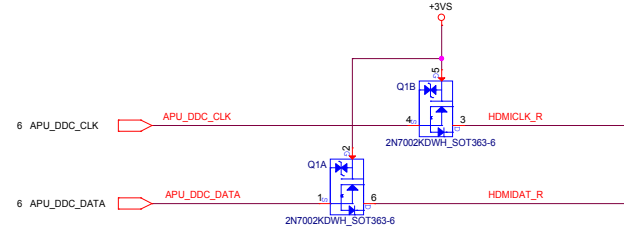
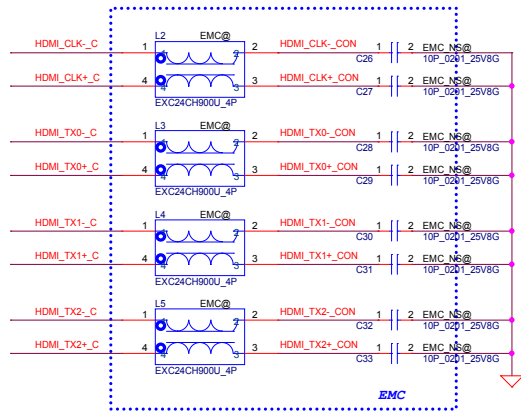
For EMI



For ESD

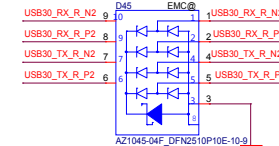
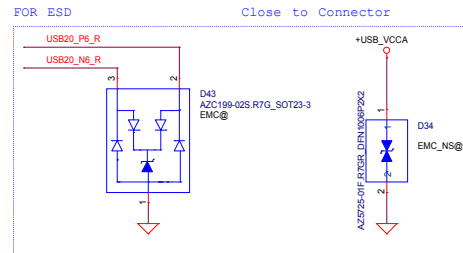
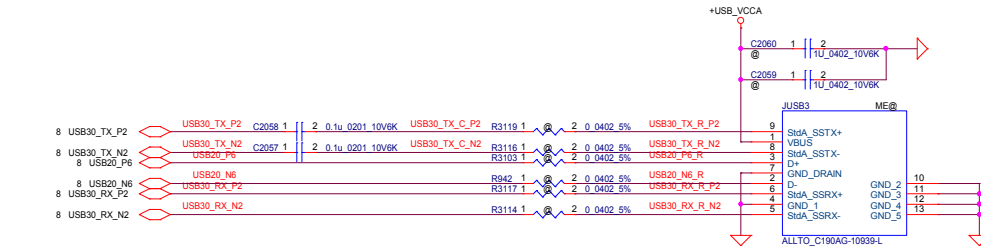
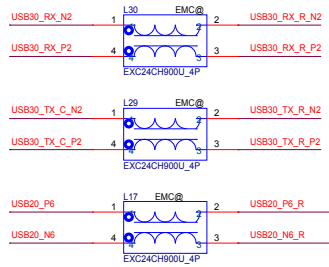
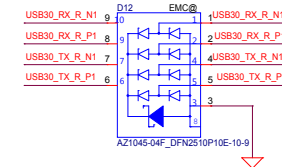
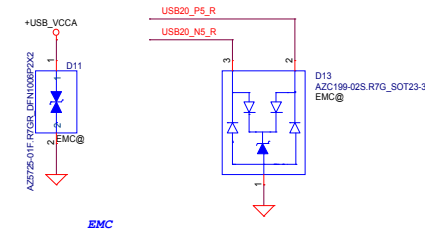
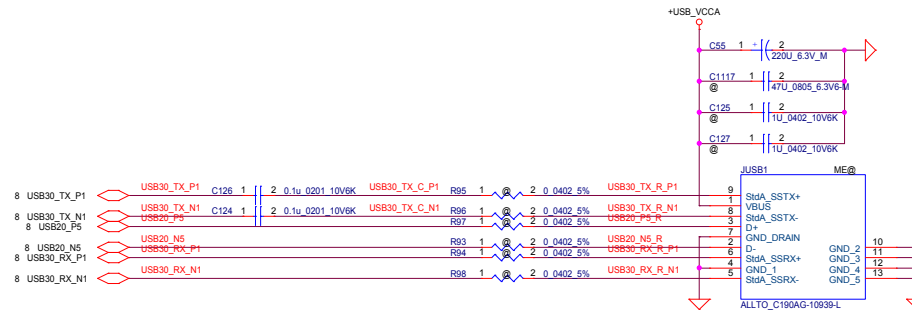
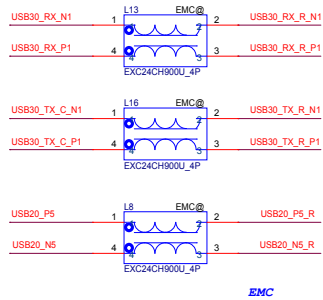
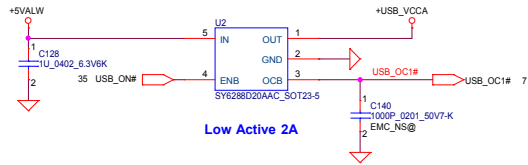


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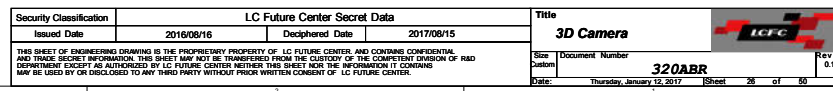
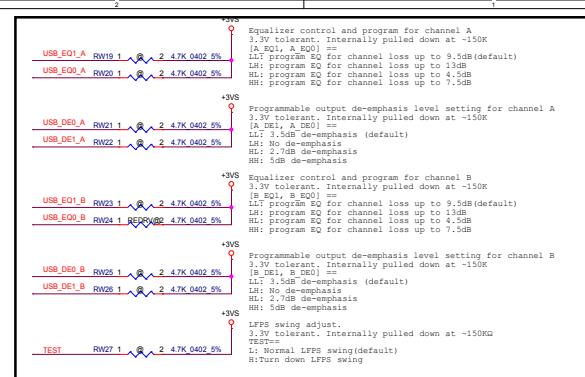


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LEFT SIDE USB3.0 PORT x2



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Date: Thursday, January 12, 2017				Sheet 25	of 50



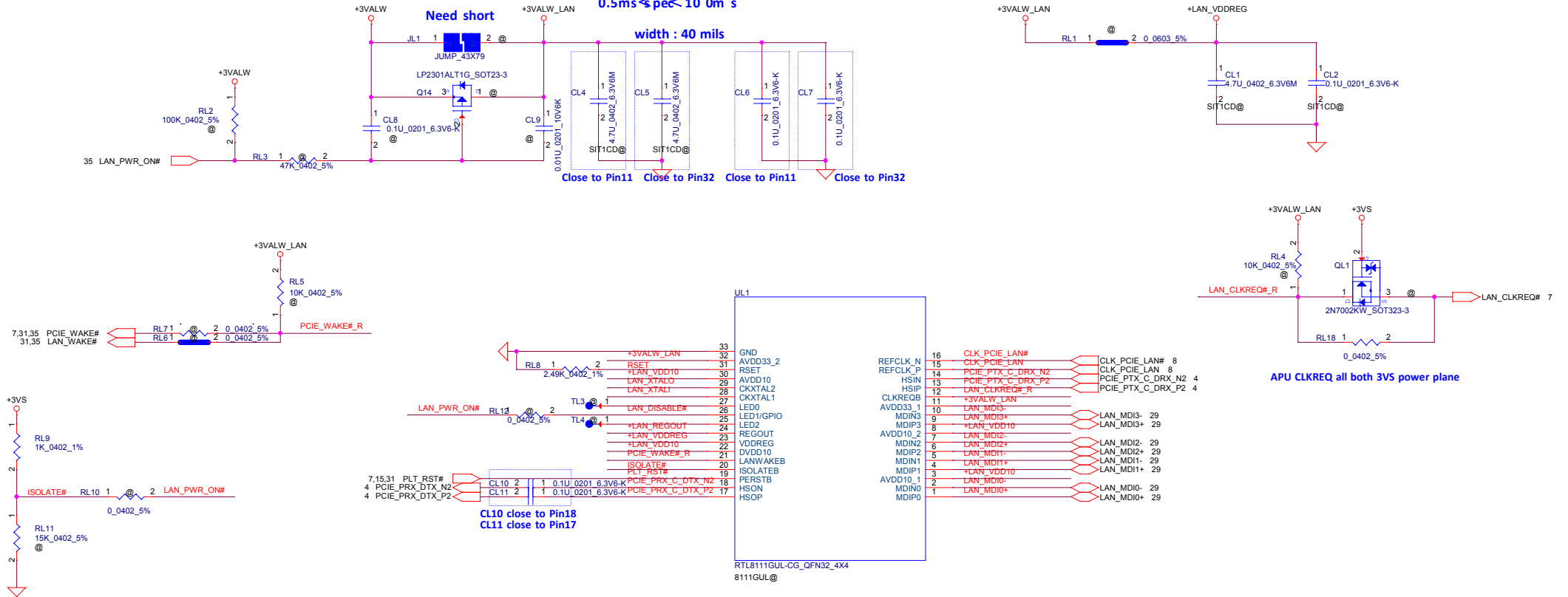
5	4	3	2	1																				
D				D																				
C				C																				
B				B																				
A				A																				
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Date:		Thursday, January 12, 2017		Sheet 27 of 50																				
5	4	3	2	1																				

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%)
0.5ms < spec < 10 0m s

Need short

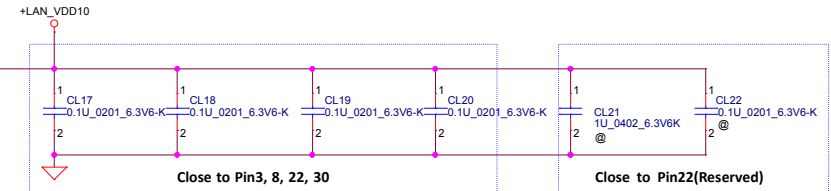
width : 40 mils




APU CLKREQ all both 3VS power plane

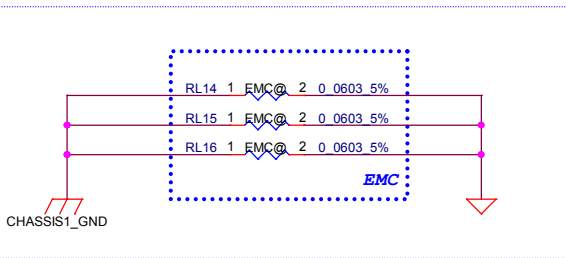
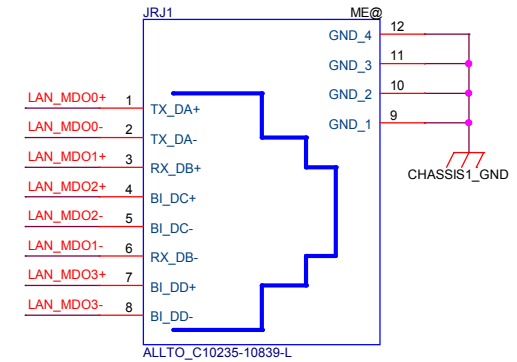
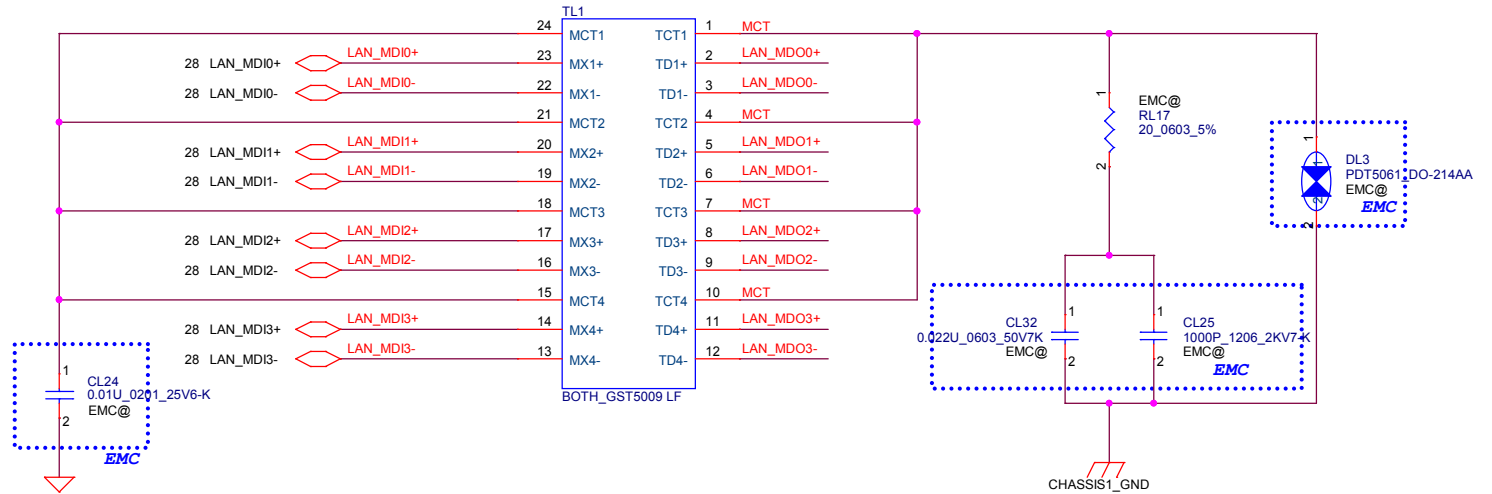
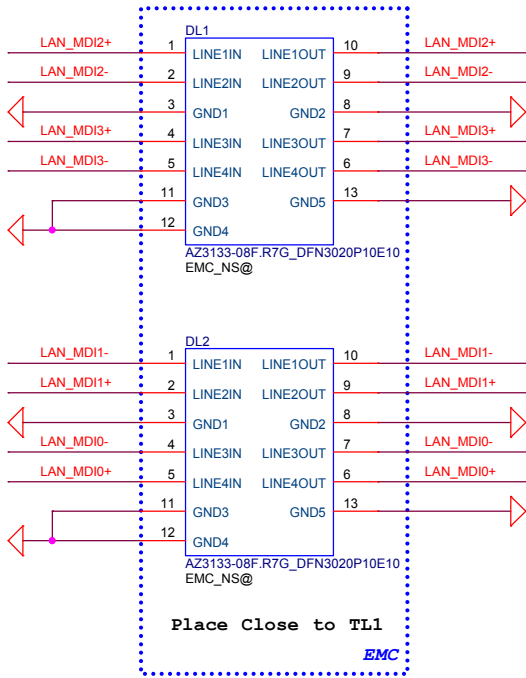
For RTL8111GUL/ RTL8106EUL (SWR mode)
For RTL8111H (LDO mode) RL19 stuff

Layout Note: LL1 must be within 200mil to Pin24, CL15, CL16 must be within 200mil to LL1
+LAN_REGOUT: Width = 60mil

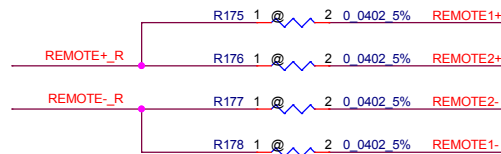
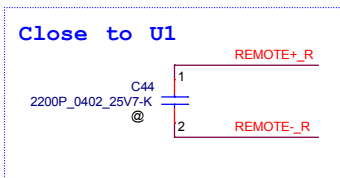


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Date:		Thursday, January 12, 2017		Sheet 28 of 50		

DL1/DL2 1'S PN:SC300003M00

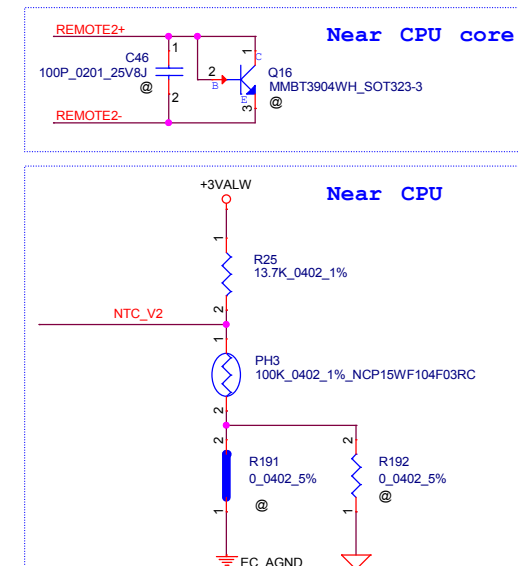
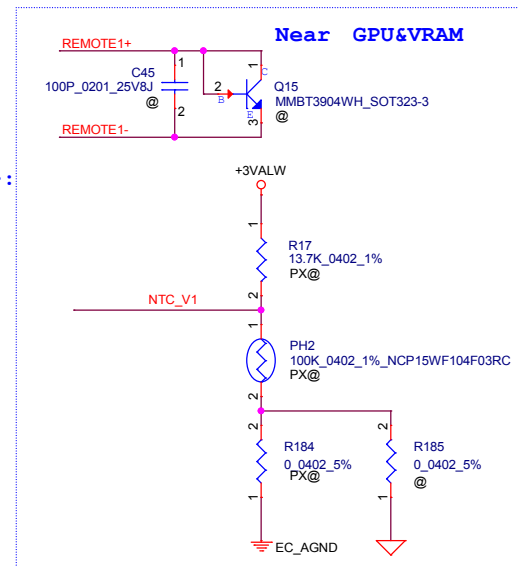
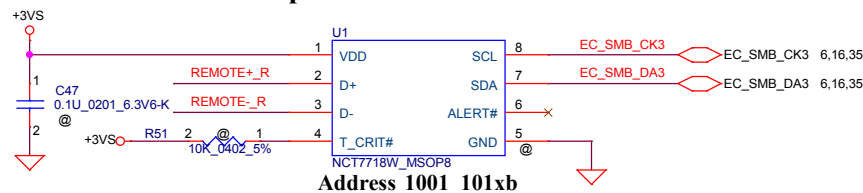


Security Classification	LC Future Center Secret Data			Title	LAN_Transformer	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size Custom	Document Number	Rev 0.1
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				Date:	Thursday, January 12, 2017	Sheet 29 of 50

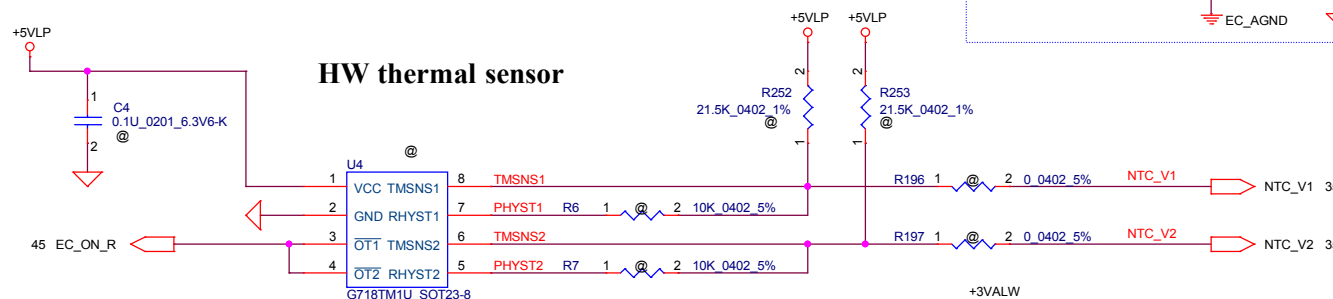


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

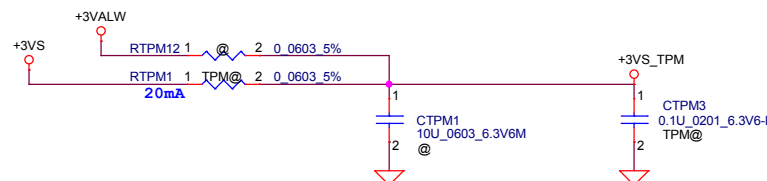
SMSC thermal sensor placed near DIMM



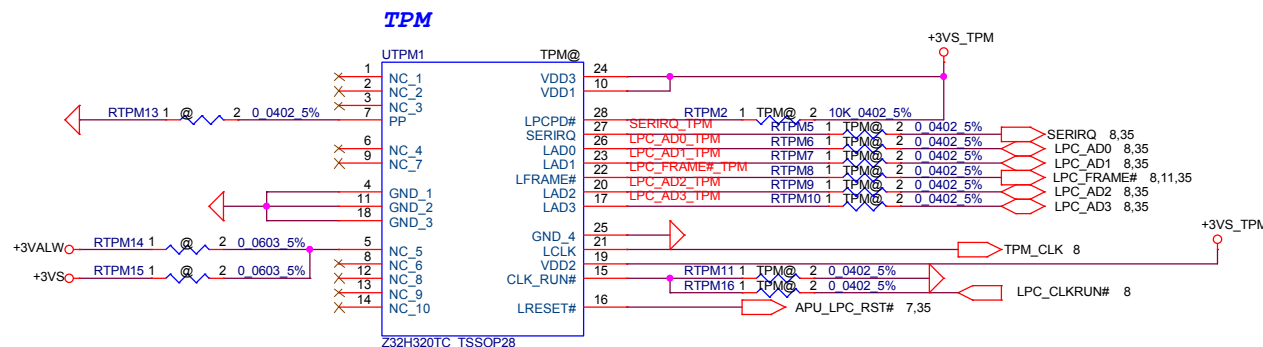
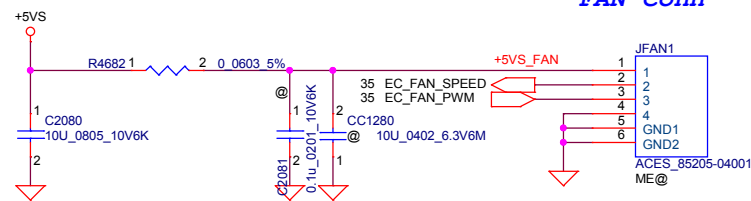
HW thermal sensor



over temperature threshold:
 $RSET=3*RTMH$
 $92+/-30C$
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
 $56+/-30C$



FAN Conn

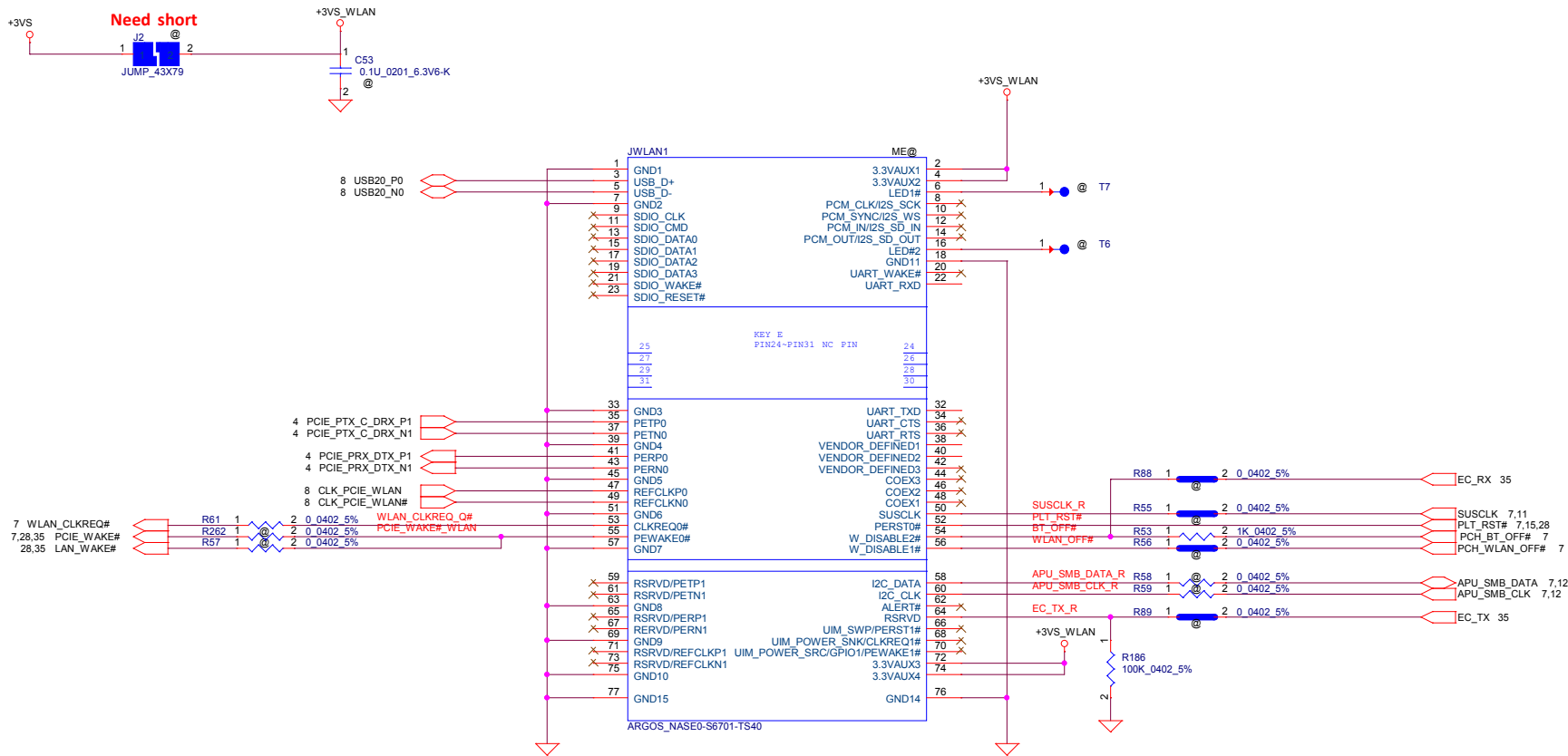


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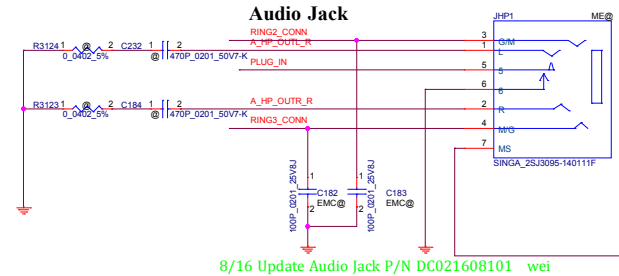
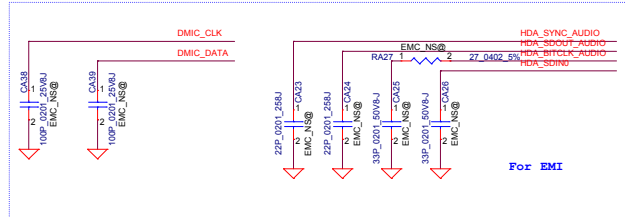
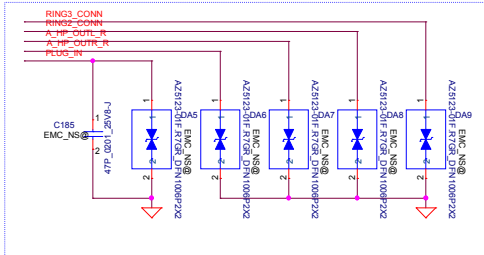
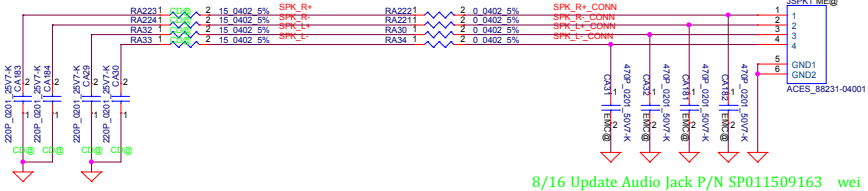
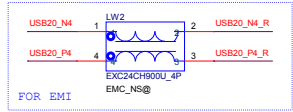
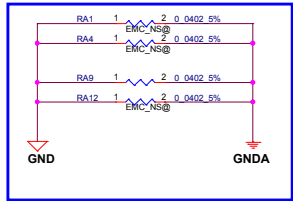
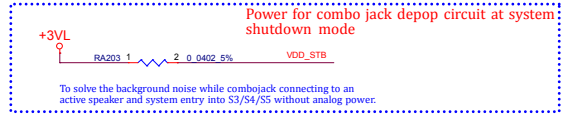
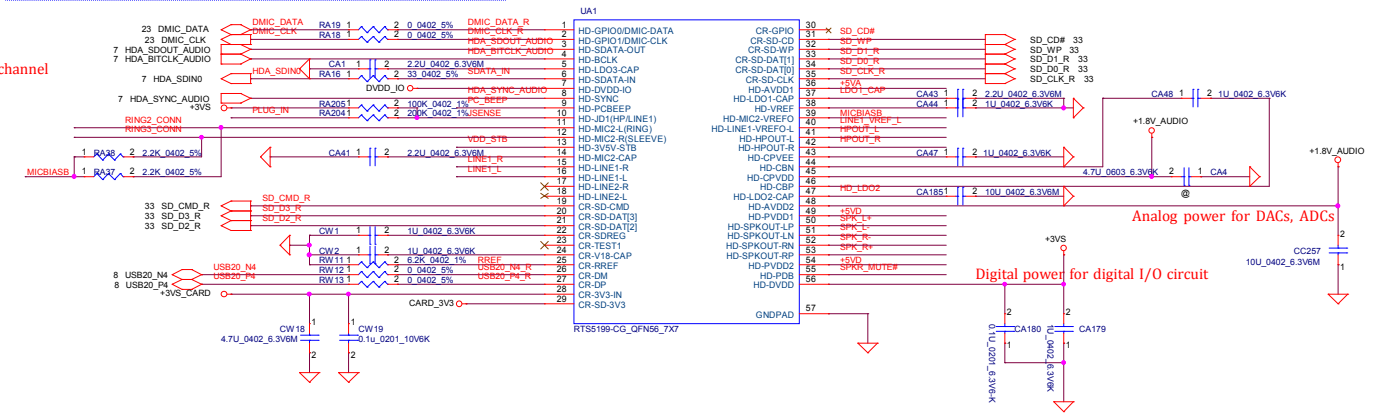
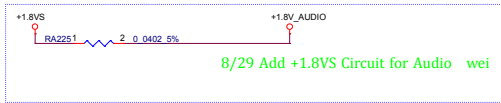
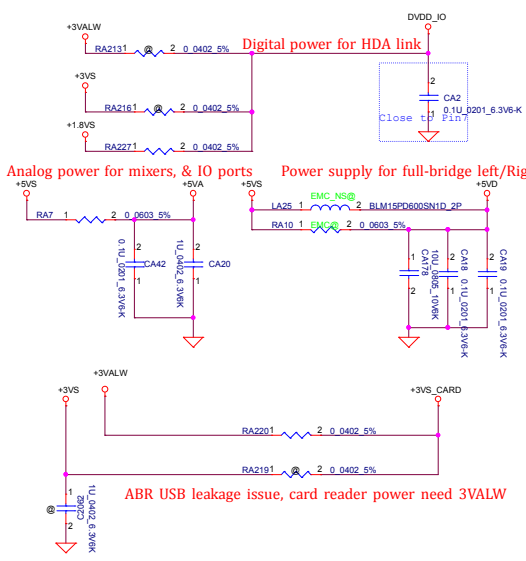
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Size	Custom
Document Number	320ABR
Date:	Thursday, January 12, 2017
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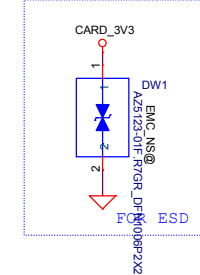
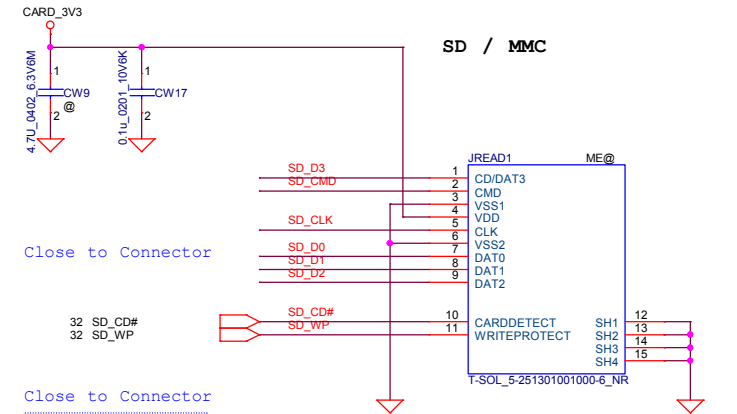
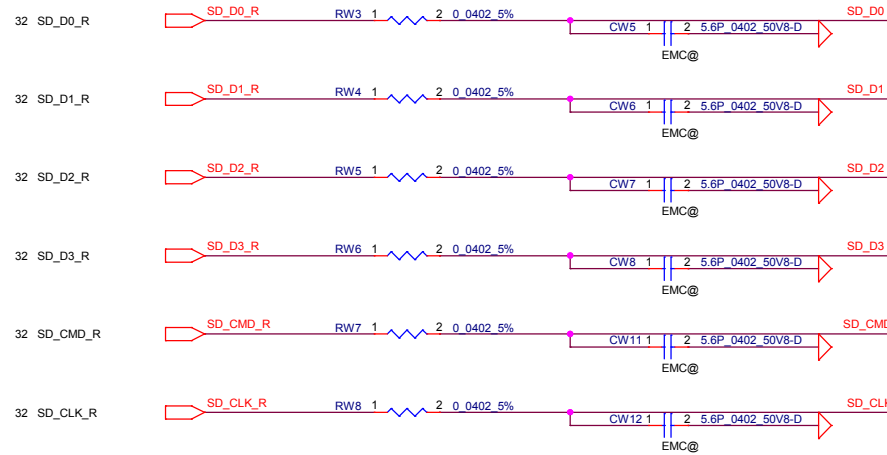
Mini-Express Card(WLAN/WiMAX)




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				320ABR	
				Rev	0.1
Date:		Thursday, January 12, 2017		Sheet	31 of 50



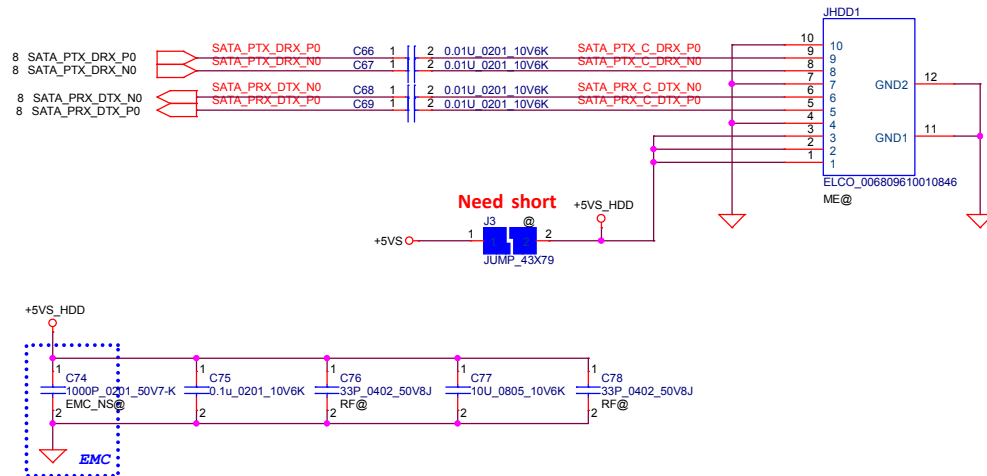
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Issued Date	2016/08/16	Deciphered Date	2017/08/15		Codec & CR_RTS5199	
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Size	Document Number	320ABR		Rev	0.1	
Date	Thursday, January 12, 2017	Sheet	32	of	50	



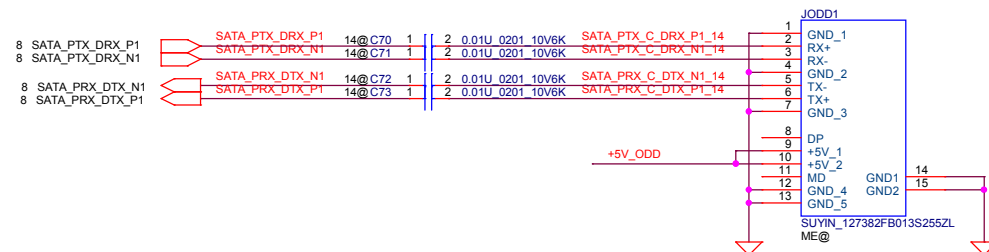
8/16 Update Conn. P/N SP07000WG00 wei

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Issued Date	2016/08/16	Deciphered Date	2017/08/15	Cardreader			
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				Custom	320ABR		
				Date:	Thursday, January 12, 2017	Sheet	33 of 50

SATA HDD Conn.



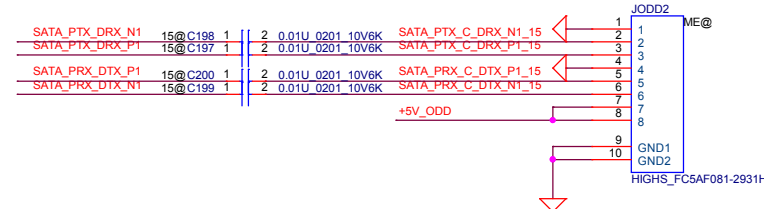
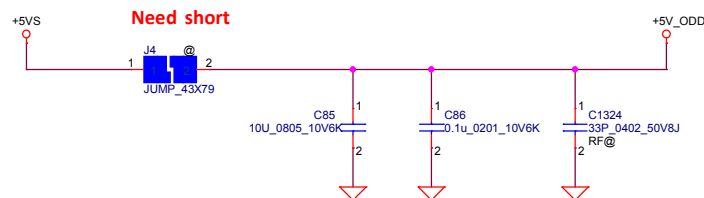
FOR 14" SATA ODD Conn.




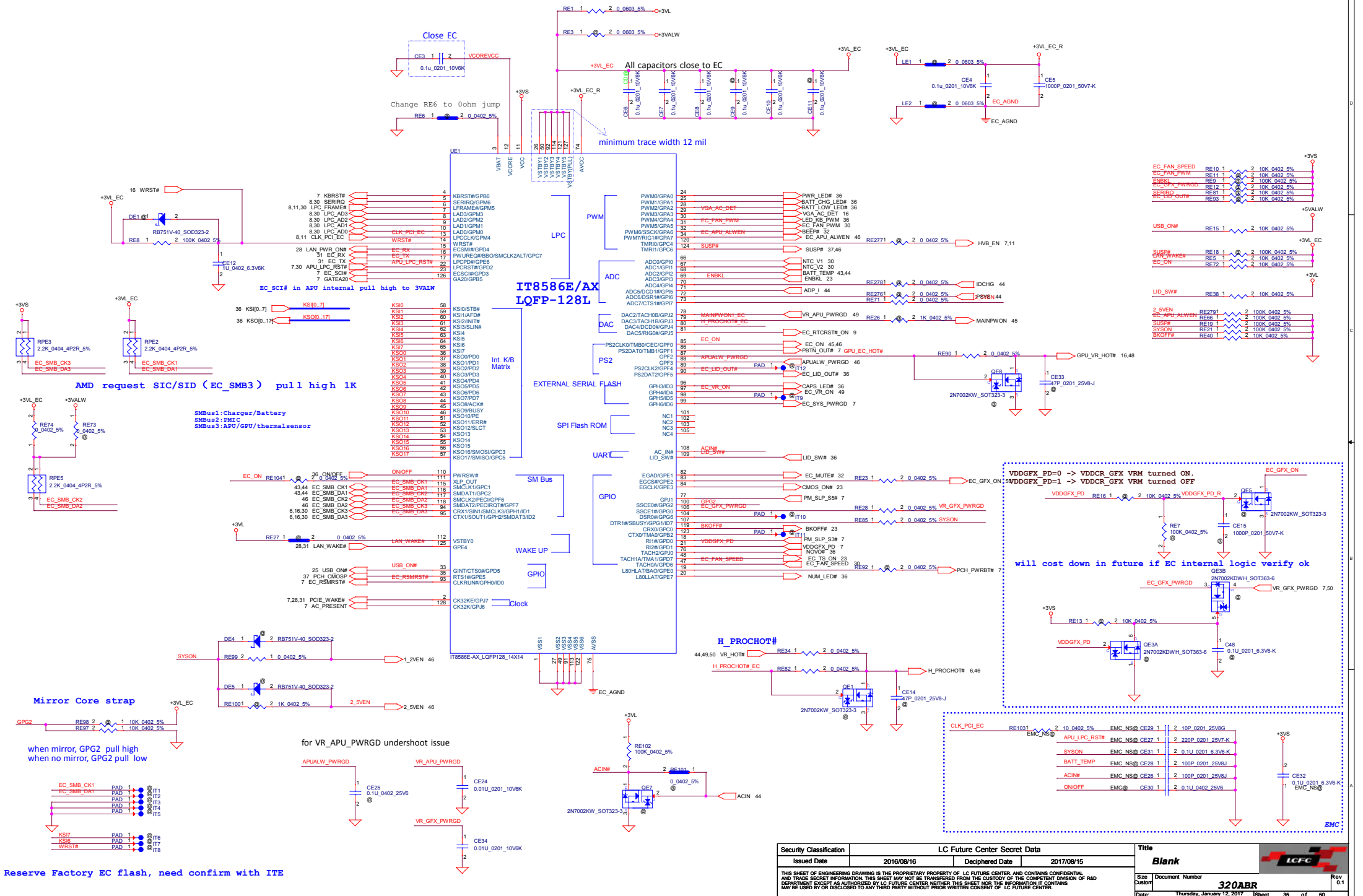
FOR 15" SATA ODD FFC Conn

SATA 15 ODD P/N pin assign is different from G SKL

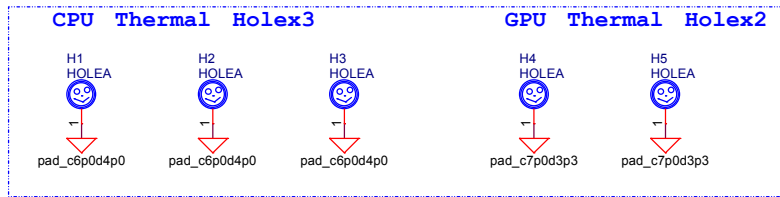
+5VS to +5V_ODD



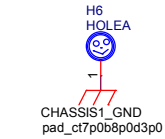
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	HDD/ODD CONN			
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Date:		Thursday, January 12, 2017		Sheet	34	of	50



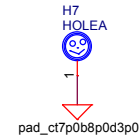
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Date		Thursday, January 12, 2017		Sheet		0.1



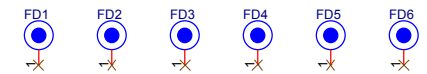
Close to RJ45



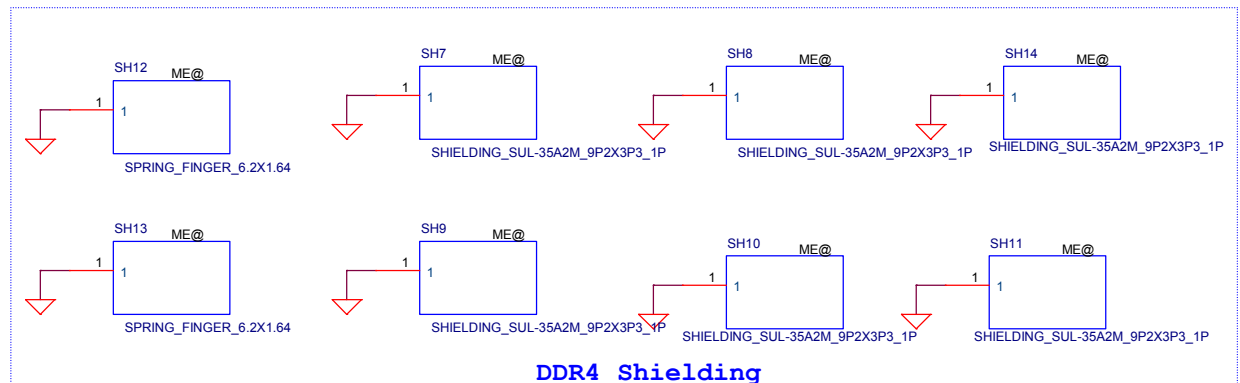
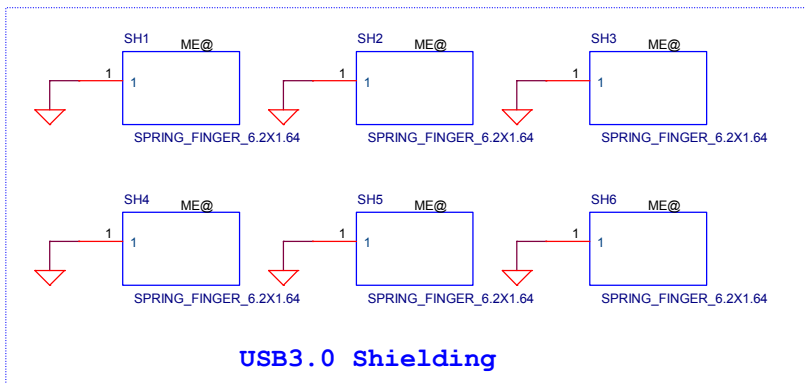
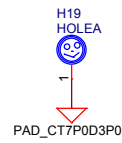
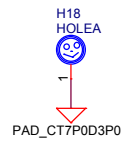
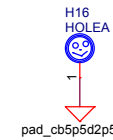
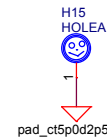
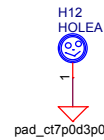
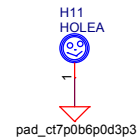
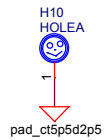
Close to Audio jack




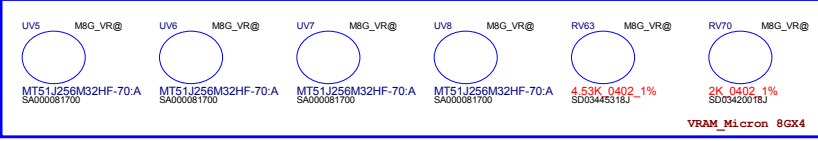
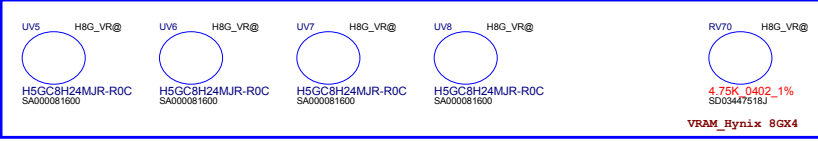
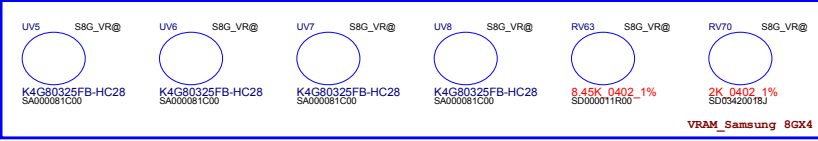
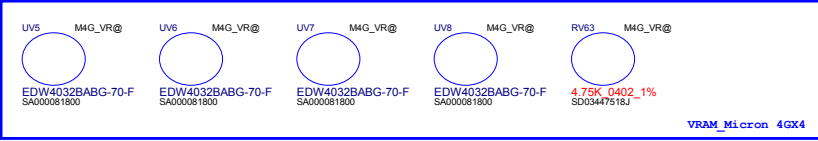
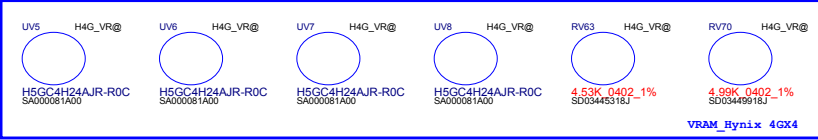
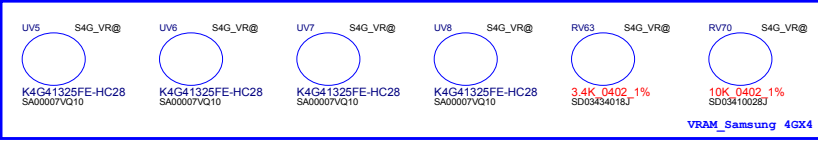
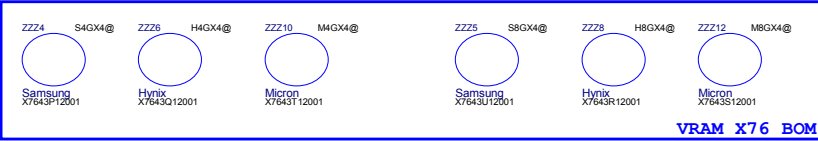
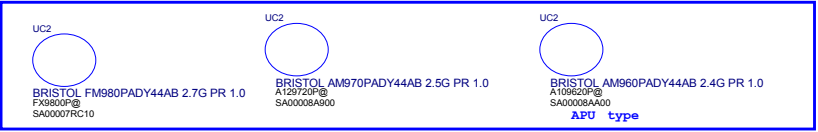
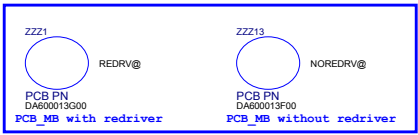
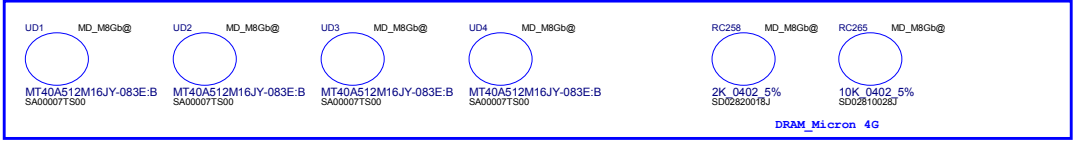
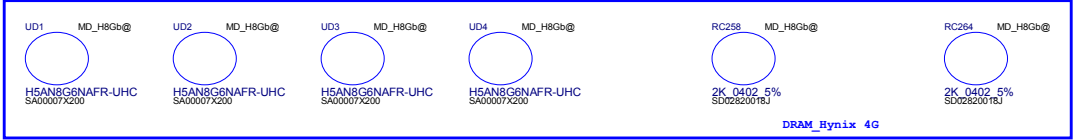
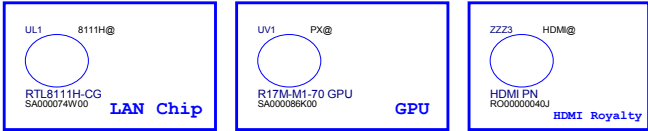
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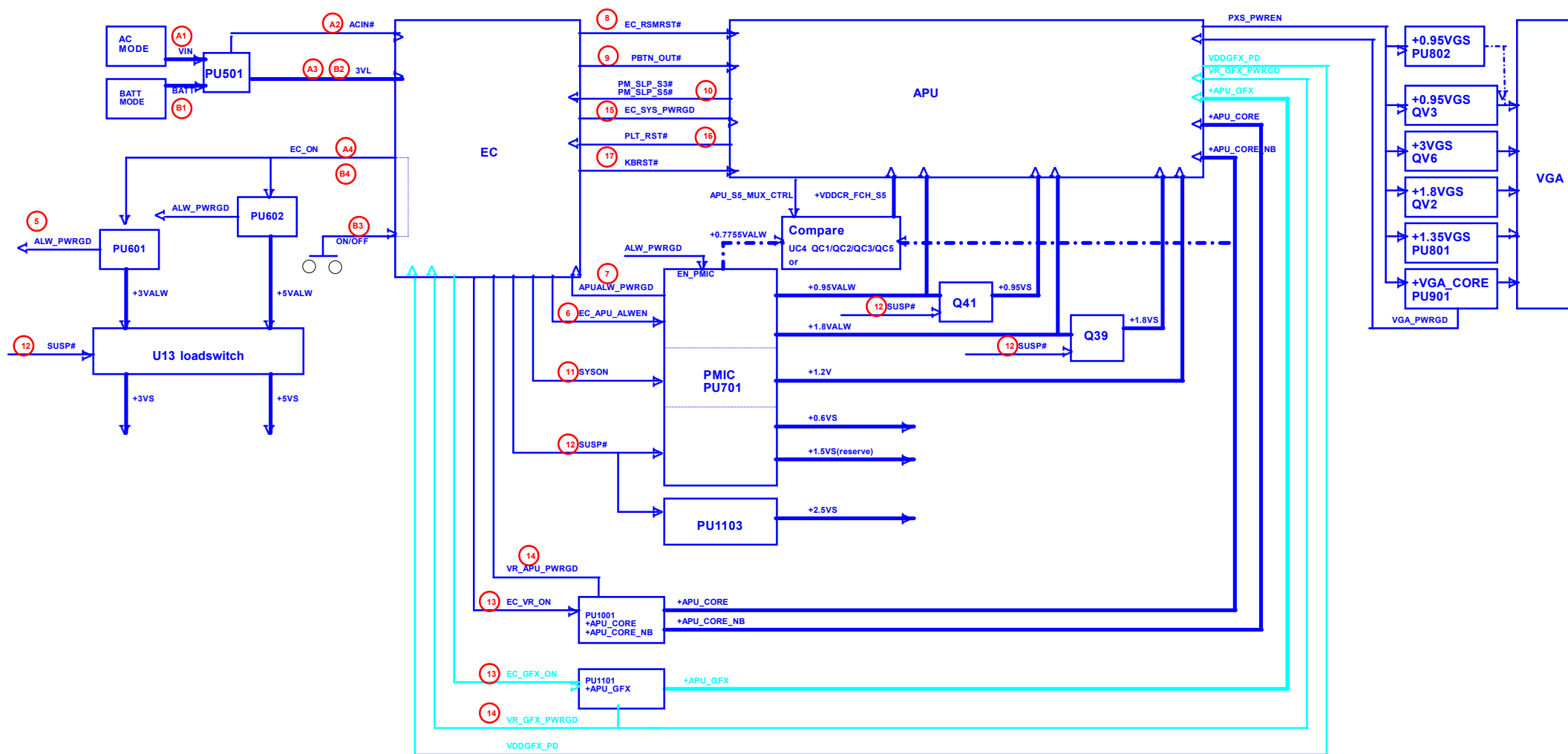


WLAN Standoff

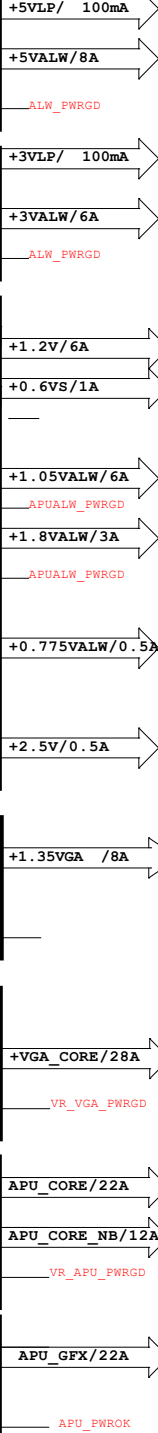
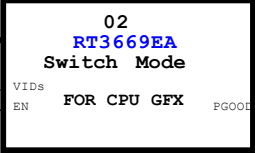
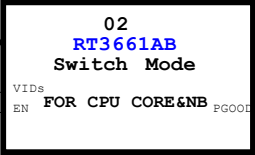
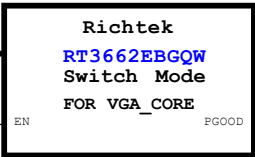
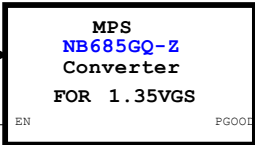
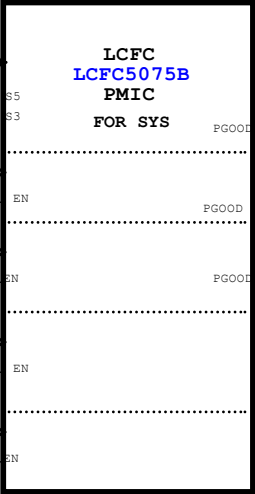
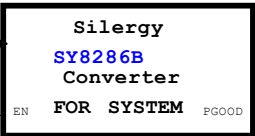
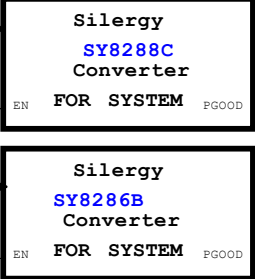
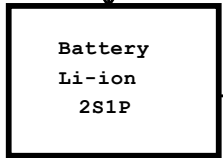
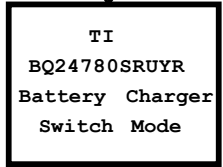



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				Date:	Thursday, January 12, 2017	Sheet 38 of 50

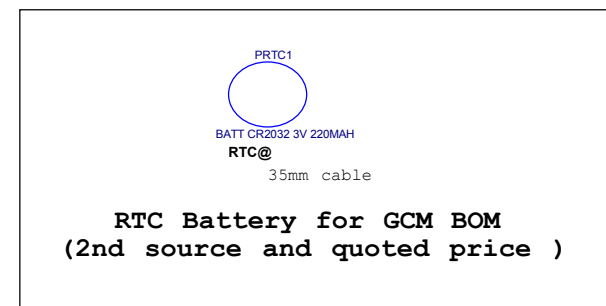
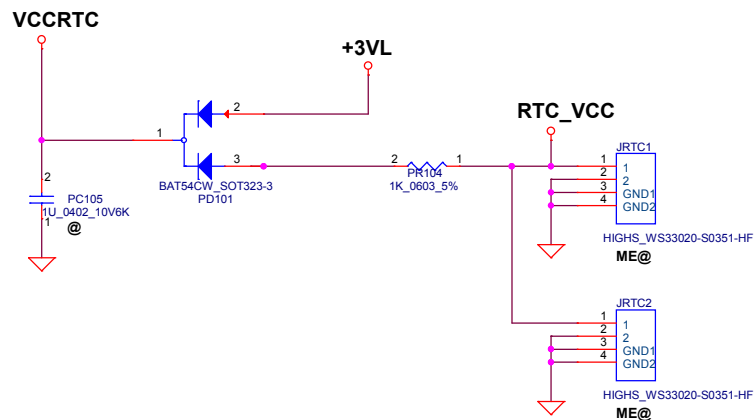
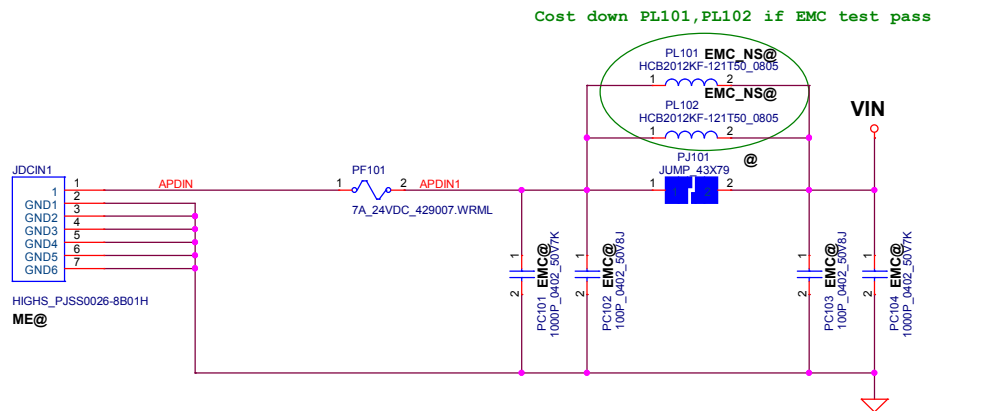





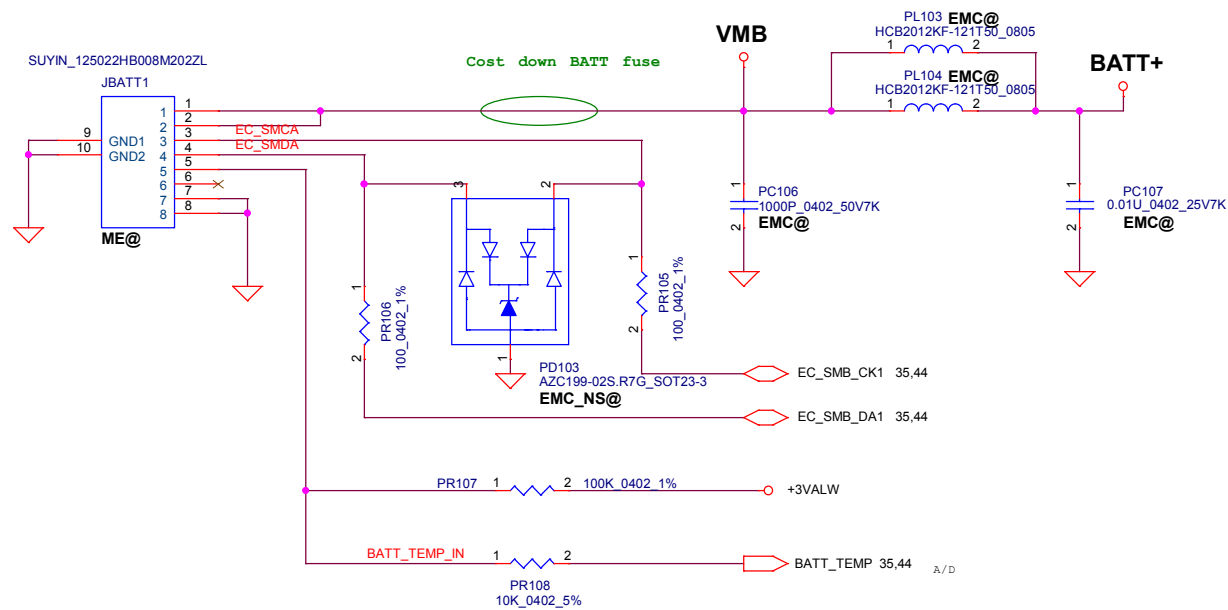
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	Power sequence Block	
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Custom					
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	Power Diagram	
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Size Custom	Document Number 320ABR	Date: Thursday, January 12, 2017	Sheet 41	of 50	

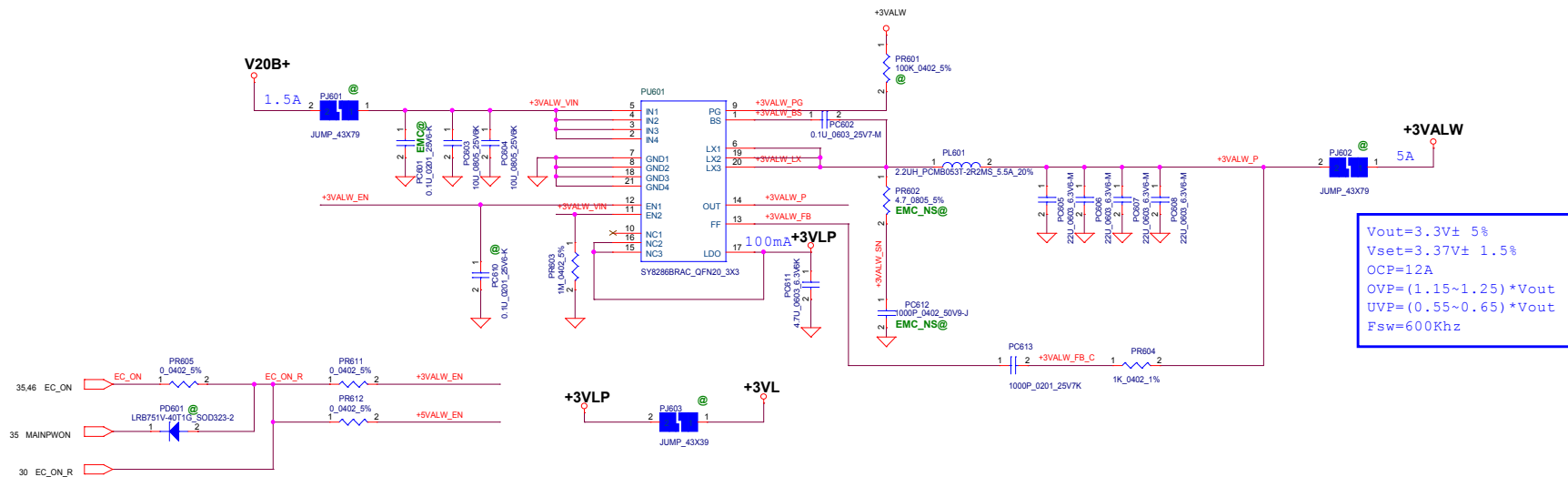


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Issued Date	2013/08/15	Deciphered Date	2013/08/15	DCIN / RTC		
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Size Custom	Document Number		320ABR		Rev 0.1	
Date:	Thursday, January 12, 2017		Sheet	42	of	50

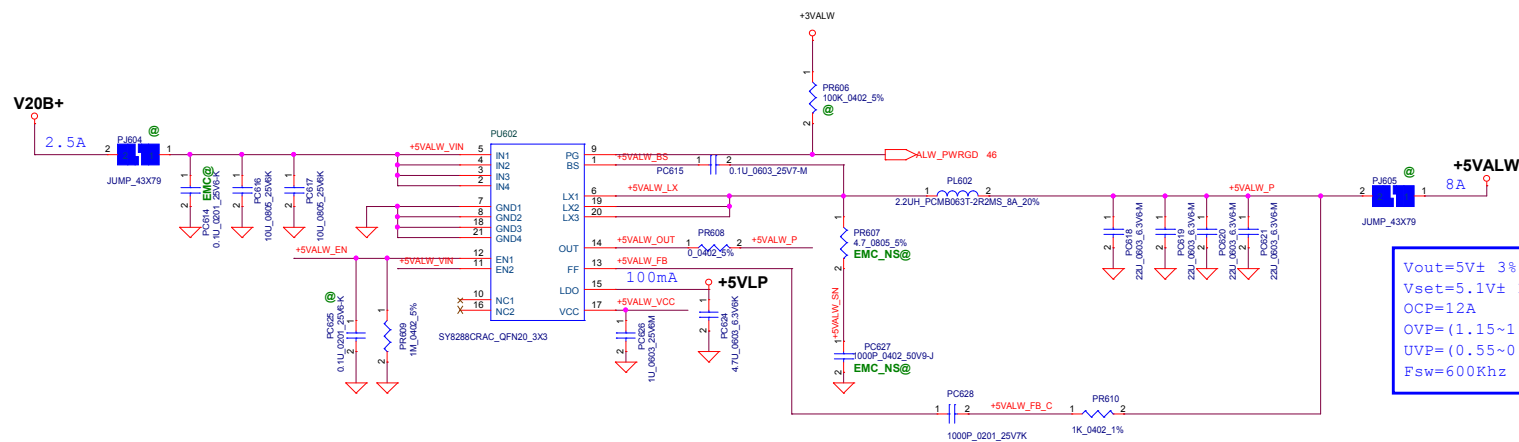


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	BATTERY CONN/OTP	
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				Document Number	0.1
				Date:	Thursday, January 12, 2017
				Sheet	43 of 50

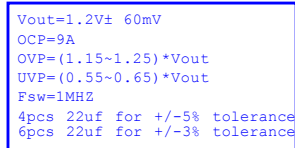




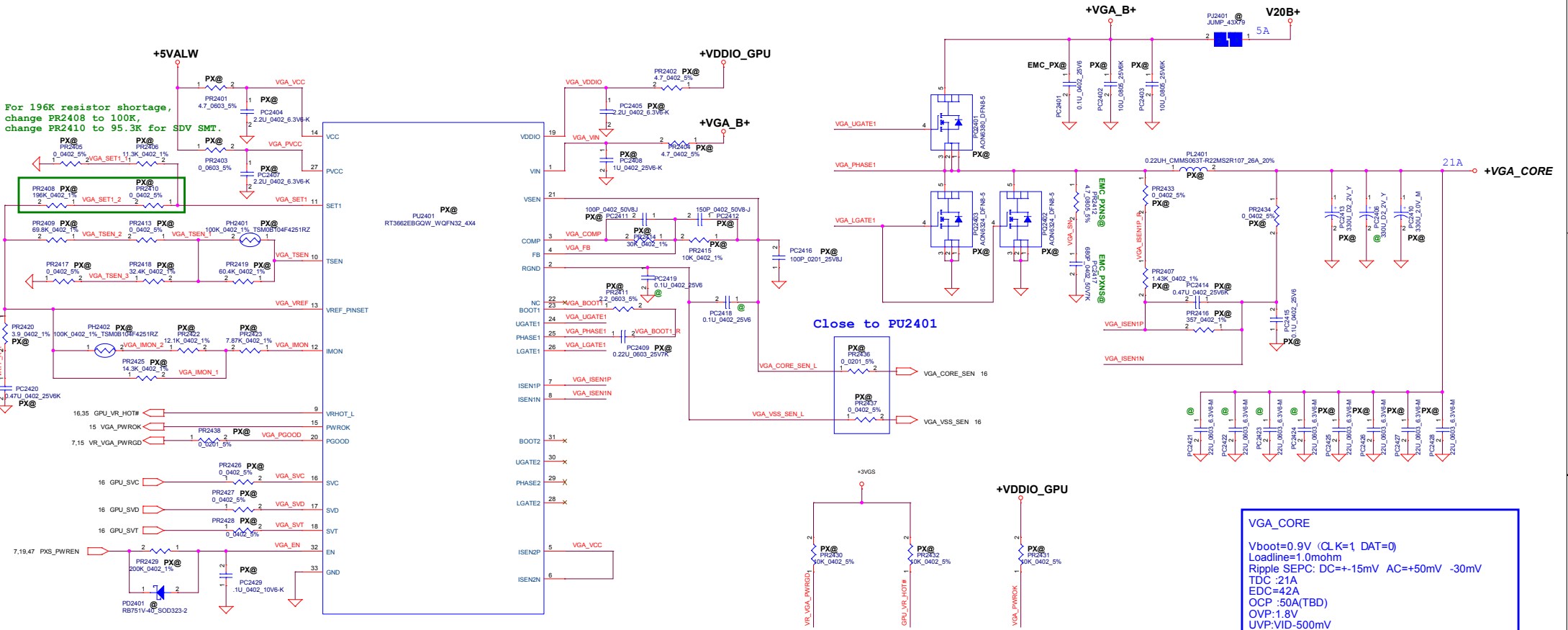
$V_{out} = 3.3V \pm 5\%$
 $V_{set} = 3.37V \pm 1.5\%$
 $OCP = 12A$
 $OVP = (1.15 \sim 1.25) * V_{out}$
 $UVP = (0.55 \sim 0.65) * V_{out}$
 $F_{sw} = 600Khz$



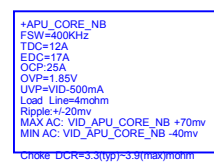
$V_{out} = 5V \pm 3\%$
 $V_{set} = 5.1V \pm 1.5\%$
 $OCP = 12A$
 $OVP = (1.15 \sim 1.25) * V_{out}$
 $UVP = (0.55 \sim 0.65) * V_{out}$
 $F_{sw} = 600Khz$



For 196K resistor shortage,
change PR2408 to 100K,
change PR2410 to 95.3K for SDV SMT.



Security Classification	LC Future Center Secret Data		Title	PWR-XXXX	Rev 0.1
Issued Date	2016/01/20	Deciphered Date	2016/01/20		
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The schematic diagram illustrates the SVID interface circuit. A +1.8VS supply is connected to a network of resistors and capacitors. On the left, three capacitors (220 pF) are connected to the supply. In the center, a network of resistors (10k, 22k, 10k, 22k, 10k, 22k) and capacitors (220 pF) is shown. On the right, a blue box labeled 'Close to SVID pull high net' contains a pull-up resistor (1.51k, 0.402, 1%) and a capacitor (100 pF) connected to the +1.8VS supply. The output signal is labeled APUL_VRL_HOT_1.

